A measurement based comparison of full-wave and quasi-static methods for baseband modeling of plated through hole via structures

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A MEASUREMENT BASED COMPARISON OF FULL-WAVE AND QUASI-STATIC METHODS FOR BASEBAND MODELING OF PLATED THROUGH HOLE VIA STRUCTURES

BY

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THESIS

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DEDICATION

To my grandparents
Simonne Lessard, Raymond Cartier, and Gabrielle Cartier
for their inspiration
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ABSTRACT

A MEASUREMENT BASED COMPARISON OF FULL-WAVE AND QUASI-STATIC METHODS FOR BASEBAND MODELING OF PLATED THROUGH HOLE VIA STRUCTURES

by

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University of New Hampshire, May 2008

As signaling rates increase, the usable bandwidth of modern telecommunication and storage systems is bounded by parasitic elements within the signal path. To improve data throughput, system designers use cascaded combinations of equivalent circuit models obtained through component level simulation and measurement to evaluate the communications channel. The analytical methods used to create these models have frequency dependent limitations and restrict applications. To this end, a measurement based comparison of quasi-static and full-wave simulation methodologies was performed on plated through hole via structures in a printed circuit board over a frequency range of 0.1GHz to 20GHz.

Test fixtures and calibration standards, which isolate the behavior of the component under test from the measurement set-up, are required to establish performance metrics used for the evaluation. In this study, a printed circuit board
was designed and fabricated to contrast two different calibration methodologies as applied to plated through hole via structures.

The results of this study will describe the usable bandwidth associated with equivalent circuit models derived from quasi-static electromagnetic simulations while demonstrating strong correlation between the full-wave electromagnetic models and measured scattering parameters of a plated through hole via structure.
CHAPTER 1

INTRODUCTION

In this chapter, a background description of plated through hole via structures is detailed. The chapter highlights the incentives for the characterization of via structures through two different types of simulation and measurement, discusses the various types of via structures, details two types of plated through hole via structure used in this study, and provides an overview of the methodologies used in the analysis.

1.1 - Background

In printed circuit boards carrying multi-gigabit per second digital signals, transmission bandwidth and data throughput are significantly limited by parasitic effects of plated through hole via structures which are used to connect surface mount or pressfit components to inner signal layers, or different inner signal layers to each other. In particular, the resonance created by via stubs will limit transmission over certain ranges of frequencies corresponding to twenty gigabit per second digital data rates. Cohen [Coh03], in a study analyzing the transmission of via stubs showed that a secondary drilling operation in the fabrication process can be used to reduce the length of the via stub. This technique increases the resonant frequency of the via structure out of the desired transmission bandwidth. However, a procedure for identifying plated through hole via stubs is required for schematic design tools used in the manufacturing process.
Harrington, Mautz, and Wang used quasi-static analysis and the method of moments to calculate the equivalent circuit parameters of a via structure connecting two transmission lines [Wan87]. The results are in the form of dimensional parameters which minimize reflections and optimize the via impedance. To extend the validity of equivalent circuits beyond 1 GHz, the number of transmission line networks used to represent a plated through hole via structure has to be increased.

Liaw and Merkelo performed an analysis of mode conversion occurring at via structures with full-wave simulation techniques [Lia95]. These full-wave simulation techniques are based on time varying Maxwellian equations rather than the static equations used in the former simulation method, which did not include the effects of displacement currents. In this thesis, no modeling approach was performed as the stripline and plated through hole via structure in the printed circuit board test fixture are too complex. Instead, the via structure was analyzed using a commercially available finite integral full-wave solver.

To understand the performance of plated through hole via structures and their impact on system performance with escalating data rates, a measurement based comparison of scattering parameters obtained from quasi-static equivalent circuits and full-wave simulation methodologies was performed. This analysis was carried out on two types of plated through hole via structure. The first type can be characterized as resonant and reflective while the second is non-resonant and well-matched. Two available simulation tools, which apply different modeling
methodologies, are used to obtain frequency domain scattering parameters of the via test structures. Simulation accuracy was substantiated by making a simple experimental set-up and measuring the scattering parameters. This comparison helped in assessing model validity and improved modeling techniques at data rates exceeding 2.5 gigabits per second. In performing this comparison, experiments were designed that included calibration structures necessary to isolate the performance of plated through hole via structures from the measurement equipment. De-embedding techniques were applied, in the frequency domain, to remove any effects created by the fixture or test equipment. This approach to measuring plated through hole via structures provided accurate data to the higher bandwidths necessary for a modeling comparison.

1.2 - Characterization

In this thesis, measurements on resonant and non-resonant experimental via structures were used to find the applicable bandwidth of equivalent circuits resulting from quasi-static and full-wave simulation. Strong correlation between simulation method and measurement indicated good modeling practices which can be applied to future via structure evaluations. Conversely, poor correlation determined the limitations of a modeling technique applied and determines the usable bandwidth for the technique.

Broadband comparisons of simulated and measured data are technically challenging. Data derived from measurement often include the parasitic effects
associated with cable attachments and other fixturing necessary for component characterization. Data derived from simulation may contain computational error sources associated with the simulation set-up, including boundary conditions, excitation sources, discretization, and background materials.

1.3 - Simulation Methodologies

A variety of electromagnetic simulation methods are available to predict the electrical performance of via structures. One category of simulation method uses electrostatic and magnetoquasi-static field solvers to derive equivalent circuit element models of the structure [Nab92]. Models derived by these methods are accurate at frequencies for structures whose size is less than an eighth of one wavelength. As the transmission delay of a typical printed circuit board plated through hole via is in the range of 20 to 50 picoseconds, the electrostatic and magneto-static field solvers can be used for frequencies ranging from 2.5 gigahertz to 6 gigahertz respectively. For this reason, the accuracy of models derived by these methods for the design of systems involving 6 to 12 gigabit per second data transmission rates calls for investigation. For this frequency range, simulation methods rely on the computation of electromagnetic fields propagating through the structure in the time domain [Sch96]. As the time domain solver makes no quasi-static assumption, this type of method is accurate to higher frequencies. The main limitation of the full-wave simulation is the availability of high-speed computational resources. However, the output of this
method is typically in the time domain or in the form of frequency domain scattering parameters. To obtain an equivalent circuit model, the full-wave simulation methodology may require an additional computational step to produce a circuit simulator compatible model [Gri]. Some circuit simulators can perform this additional step internally [Sta02]. When used to model resonant structures this method may require long simulation times.

1.4 - Measurement Analysis

An assessment of the modeling accuracy and the usable bandwidth of the contrasting quasi-static and full wave electromagnetic simulation methods, for modeling through hole via structures, was performed by comparing the modeling results to measured data. Data for this comparison was obtained from specially constructed printed circuit boards. These printed circuit boards are composed of FR-4 epoxy glass composite insulating layers alternating with eight conductive layers of copper (two outer pads-only layers on layers one and eight, four ground planes on layers two, four, five, and seven, and two 50 Ohm characteristic impedance stripline signal layers on layers three and six). The test boards included a set of on-board equivalently fixtured standards to allow a wideband TRL [Poz05] calibration/de-embedding technique to be applied in the frequency domain. Calibrated measurements were taken on a Vector Network Analyzer (VNA) over the range of 100 MHz to 20 GHz. In addition, direct time domain measurements of reflection and transmission were taken using TDR [Agi04] test
equipment at a 30 picosecond step risetime. This risetime provided a digital knee frequency [Joh93] of 16.67 GHz.

1.5 - Types Plated Through Hole Via Structure

Plated through hole via structures may be categorized as non-resonant and resonant. The first type of plated through hole via used in this analysis is a pass-through via structure that connects an input stripline trace on an upper signal layer in the printed circuit board to an output stripline trace on a lower signal layer in the printed circuit board. The second type is a stub via structure for which the input and output stripline traces were both on the upper signal layer in the printed circuit board, creating a stub.

1.6 - Organization

Chapter II presents the measurement techniques used. It will also include the design of the fixture, measurement calibration, and error sources in the measurements. Chapters III and IV will describe the quasi-static and full-wave modeling approaches used in this study. Chapters III and IV also reduce the techniques used in modeling the plated through hole via structures to practice. This includes verification against closed form solutions, establishing limitations within the tools themselves, sources of error in the models, and lessons learned from applying the simulation tools to a via structure. Chapter V describes the
lumped element model derived from the quasi-static electromagnetic simulation technique. In this derivation, an appropriate method of separating the plated through hole via structure into lumped elements (capacitances, inductance, etc) was determined. Chapter 6 presents the results of the modeling. Data resulting from the simulation were compared with calibrated measurement data. And Chapter 7 is the analysis of the results, including conclusions, and suggestions for future areas of work.
Chapter 2 describes in detail the fixtures which were created for this study and the calibration techniques that were employed to produce accurate measurement results. It emphasizes the design process for the test fixture, which structures were incorporated into the fixture, how the fixture was fabricated, the motivation for calibration structures, the calibration techniques applied in this study, and how the calibration structures apply to plated through hole via structures.

2.1 - Fixture Design

A fixture is defined as an experimental structure built to isolate the electrical network parameters of a device under test from measurement equipment. The goal of the fixturing used in this study is to separate a plated through hole via structure from the vector network analyzer (VNA) or time domain reflectometer (TDR). This isolation is achieved through an RF quality test fixture. While a number of different approaches could be taken to create a test fixture, a printed circuit board based fixture was used in this body of research. Typically, plated through hole via structures are used in laminated fiberglass epoxy resin style layered printed circuit boards. This makes printed circuit board test fixtures favorable over RF fixtures created by scaled approximations. The printed circuit boards constructed for these measurements were composed of FR-4 epoxy glass composite insulating layers alternating with eight conductive layers of 30 micron thick copper. As shown in Figure 1, grounded layers in the printed circuit
board were on layers 2, 4, 5, and 7, while layers 3 and 6 were 50 Ohm characteristic impedance stripline signal layers.

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**Figure 1: Printed Circuit Board Test Fixture Stack-Up**

The via structure in both pass-thru and stub type experimental cases was a cylindrical center conductor with a diameter of 305 microns, the outer and inner layer signal pads were 610 microns in diameter, and the anti-pad ground layer clearances were 1524 microns. The via test structure was located in the center of four cylindrical conductors attached to grounded layers 2, 4, 5, and 7. These grounded conductors were placed on a 3606 micron rectangular grid as shown in Figure 2.
Figure 2 - Plated Through Hole Test Vehicle Lay-Out

The plated through hole via structures created in this printed circuit board test fixture were created by connecting the inner layer 50 Ohm characteristic impedance stripline traces on layers 3 and 6 to the plated through hole via structure. Different layer combinations will produce both resonant and non-resonant via structures. In this study, a stripline trace on signal layer 3 and signal layer 6 were connected to a plated through hole via to produce the pass-through style via. This combination is illustrated in Figure 3 with both dielectric and ground layers removed for clarity.
In the resonant style of plated through hole via structure shown in Figure 4, a stripline signal trace on layer 3 was connected to a plated through hole via, which also attached to another stripline on signal layer 3. Although this single-layer-connected stub via structure was not one that would be used in a practical system board, its behavior represented an example of the important resonant stub type of via structure.

Once the structure under test had been created, the fixture needed to be updated with additional microwave quality components to attach the test
structure to the test equipment being used to evaluate the via test structure. The test connections required in this study, called for SubMiniature version A cable connectors (SMA). One style of commonly used SMA connector is a Molex SMA connector, part number 73251-1850. Equally important to the quality of the SMA connector used was the connection between the connector and the printed circuit board. Appendix A describes the inner layer details of the attachment and includes dimensions of the manufacturer's recommendations of the part used.

The lay-out of the finalized printed circuit board test vehicle is shown in Appendix B. This test vehicle includes calibration structures discussed in section 2.2 and multiple variations of plated through hole test structures. The test vehicle was fabricated at Coretec Inc.'s Toronto facility. The measurements were taken on an Optical Gauging Product. The strong magnification capabilities of the scope allowed for the very fine details of the printed circuit board to be viewed. Interestingly, the direction and size of the bundled fiberglass weave that make up the printed circuit board could be seen and also introduce a potential source of error as the epoxy resin to fiberglass ratios change at the plated through hole via structures. This change in ratios may have had an effect on the dielectric constant of the dielectric used in the printed circuit board because fiberglass and the epoxy used in the lamination process do not have consistent dielectric constants.
2.2 - Motivation For Calibration Structures

The test signal connections used to attach the plated through hole via structures to the test equipment presented a significant issue in any correlation study between measurement and model. While the SMA connectors used were high quality microwave parts, they still introduced error when measured with a Time Domain Reflectometer (TDR) or Vector Network Analyzer (VNA). As conceptualized, the SMA, connector itself is limited to a bandwidth of 18GHz. Recent advances in modeling techniques and production machining have introduced variations on the original SMA allowing for bandwidths greater than 20GHz. Unfortunately, the band-limiting nature of the SMA was difficult to compensate for in measurement, especially if the SMA was allowing modes other than the quasi-transverse electromagnetic mode of energy to propagate.

Additionally, the plated through hole via test structures were attached to stripline traces within the printed circuit board which were required to be attached via structures being tested to the measurement instrument interface. The additional stripline trace in the printed circuit board and SMA cable attachment gave rise to attenuation and increased reflections. These additional components became a part of the device under test and influence measurements taken on the test structure. Calibration and de-embedding techniques were used to remove the parasitic effects of the SMA and stripline.
2.3 - SOLT Frequency Domain Calibration

The first and most basic type of calibration used in this study was a Short Open Load Thru (SOLT) calibration. SOLT calibration moved the measurement plane to the end of the test cables. This calibration process compensated for impedance mismatched switches, couplers, and receivers in the front end of the vector network analyzer, as well as the cables used to connect the front end of the vector network analyzer to the device under test. To achieve an SOLT calibration, a known standard was attached to the end of the test cable and measured. The measured value of the standard was then compared with the calibrated value of the standard. SOLT calibration did not compensate for the SMA test signal connections in the printed circuit board test fixture or the additional stripline etch used to connect the SMA signal launch into the plated through hole test structure under test.

By moving the measurement plane to the end of the cables, SOLT calibration provided insight into the entire fixture under test and was useful for troubleshooting fixturing errors. For example, frequency domain SOLT calibrated data may be transformed to the time domain by means of a Fourier transform (or other time domain transform algorithm), when the transformed data are inspected. The entire test fixture was viewed rather than the specific plated through hole via structure under test. Any variations created by the manufacturing processes were exposed and were corrected before the data were analyzed.
2.4 - TRL Frequency Domain Calibration

The second type of calibration technique applied in this study was the Thru, Reflect, Line (TRL) calibration. TRL was developed through signal flow analysis as a method to move the measurement plane closer to the device under test and away from the ends of the test signal cables. This reference plane shift was achieved by generating error terms associated with test fixturing. A block diagram representing the vector network analyzer measurement of a 2-port device (including error boxes) is shown in Figure 5.

![Block Diagram of TRL Calibration](image)

**Figure 5 – Fixturing Error Term Diagram**

For the plated through hole via test vehicle, the error boxes represent the SMA signal connections into the printed circuit board and the additional stripline transmission line in the test structure. It has been shown [Poz05] that the scattering parameters of these error boxes can be determined by characterizing a thru standard, a reflect standard (short), and multiple insertable lengths of transmission line. The vector network analyzer used in this study validated...
internal software features which apply the TRL calibration procedure to the plated through hole via test structure and in doing so, determined the fixturing error terms [Agi04].

Line standards used in the TRL calibration have an associated measurement bandwidth over which they can be used in testing. Therefore, multiple line length standards should be applied to cover the measurement bandwidth of interest. Measurements being taken with roughly 20GHz of bandwidth required at least three line standards (more if the lower frequency range of interest extends below 100MHz). The usable bandwidth for these standards is determined by the corresponding phase for the standard. It has been shown by Agilent Technologies that the recommended range of phase values for a line standard of is between twenty and one hundred sixty degrees of phase [Agi99]. So, the three line standards with lengths of 0.1in, 0.4in, and 1.6in, used in this study, had bandwidths of 3.15GHz to 25.2GHz, 0.789GHz to 6.31GHz, and 0.197GHz to 1.58GHz.

2.5 - Frequency Domain Limitations

In TRL measurements, the error box matrices are reciprocal and include the characterization of a single fixture with an insertable line standard. It is not feasible for the plated through hole test via to be inserted into a printed circuit board test fixture. The internal layers within printed circuit boards can not be altered without damaging the fixture once the printed circuit board has been
laminated. This fact makes it difficult to apply TRL calibration to a printed circuit board. The experimental method of using a printed circuit board for TRL calibrations includes multiple lines which include the known lengths for the line standards. Each of the transmission line structures used in the calibration has identical SMA signal jacks and printed circuit board interfaces. However, this is not the same as having a single fixture with an insertable standard. Each of the SMA signal jacks has manufacturing tolerances, the printed circuit board epoxy to resin ratio can change over a length of stripline, the impedance of the stripline itself can vary due to manufacturing tolerances, and the physical relationship between the direction of the stripline transmission line and the direction of the glass fibers used in the weave can influence the calibration.

As the length of the line standard necessary for the TRL calibration process increases with decreasing frequency, the 20MHz line standard increased to an unrealistic length. For this reason, an adjustment was made to the lower limit of the frequency range associated with the 1.6in line standard, allowing a measurement at ten degrees of phase or 0.100GHz.

2.6 - Frequency Domain Measurement Equipment

The vector network analyzer used in this study was an Agilent Technologies PNA series 4-Port vector network analyzer. Measurements were performed at Amphenol-TCS's Nashua facility.
2.7 - Time Domain Calibration

Time domain measurements of the plated through hole test via structures were taken on a Time Domain Reflectometer (TDR). Time domain reflectometry involves the measurement of reflections created by impedance mismatches along a transmission line structure.

TDRs are useful in measuring any kind of transmission line structure. They illustrate the impedance changes of the entire system under test and help determine where any significant issues may be in the test fixture. Calibration of the TDR involves normalizing the impedance of the TDR itself and then establishing a measurement plane or reference plane. In this series of experiments, this plane was the relative location of the end of the test cables used to attach the TDR sampler to the plated through hole via test fixture. The calibration is performed on the test equipment by normalizing the TDR test head itself to fifty ohms. A known fifty ohm standard is attached to the test head and the expected values of reflection are compared to the measured values of reflection created by the load standard. Any variations are compensated for internally in the TDR. Then to establish a measurement plane, the test cables are attached to the TDR head. A load and reflect standard are placed at the ends of the cables and the TDR is able to distinguish between the test cable transmission line connecting to the device under test and the device itself. This means that the TDR measurements will include the SMA signal connection into
the printed circuit board and the additional stripline transmission line in the printed circuit board.

2.8 - Time Domain Measurement Equipment

The time domain reflectometer used in this study is an Agilent Technologies 54754A TDR. Measurements were performed at Amphenol-TCS's Nashua facility.

2.9 - Time Domain Measurement Limitations

The time domain measurements used in this study are limited by the instrument calibration process, which places the measurement plane at the end of the test cable. The 50Ω load standard used to calibrate the instrument is critical in determining the impedance match of the test head in the TDR itself. In this series of experiments, the standard used is considered a metrology grade standard with an impedance variation of +/- 0.1Ω and has an upper frequency limit of 23GHz.
CHAPTER 3

MEASUREMENTS

Chapter 3 details the measurement analysis of two types of plated through hole via structure. The chapter highlights the equipment and measurement techniques applied in the frequency domain analysis of plated through hole via structures, and consequently, provides the scattering parameters used for model comparison. TDR analysis is also provided to delineate the test fixture and highlight potential error sources arising from multiple impedance discontinuities.

3.1 - Frequency Domain Measurements: Short Open Load Thru Calibration

Figure 8 illustrates the SOLT calibrated vector network analyzer measurement of $S_{21}$ for the pass-thru type plated through hole via versus the stub type plated through hole via. In comparison, the stub type via exhibited a strong resonance 15.5GHz, which was not measured in the pass-through style via case. This frequency corresponds to a quarter-wave resonance for the 1371 micron length of the shunt portion of the plated through hole via in an FR-4 dielectric.
Figure 6 – S21, SOLT Calibration

In the stub type plated through hole via structure, the stub is a parasitic shunt element attached to a transmission line. The portion of the stub which is not attached to the transmission line is an open circuit. This open circuit reflects any current (or energy) back towards the transmission line. The phase of the reflected energy changes with frequency, and at specific frequencies, the phase of the reflected energy is reversed from the original signal creating an energy minimum (null). In summary, plated through hole via structures which have a portion of the via that is not in the direct signal path have frequency dependent reactive elements, which form a resonance at a particular frequency. These stub type plated through hole via structures are not be suitable for backplane systems with bandwidth requirements past the resonance frequency.
The high frequency combing seen in the SOLT measurements is consistent with the interaction between the test fixture SMA at the end of the cable and the impedance mismatch at the front end of the vector network analyzer. The $S_{11}$ SOLT calibration reflection term for each via structure is shown in Figure 9.

![Figure 7 - S11, SOLT Calibration](image)

The reflection terms for the stub type plated through hole via structure are significantly higher than the reflection terms for the pass-through style plated through hole via. This is complementary to the transmission response because the stub type plated through hole via structure is a highly reflective resonant structure as shown by the $S_{21}$ data shown in Figure 8. The SOLT calibrated $S_{11}$ data also exhibit the high frequency combing that was expressed in the transmission data.
3.2 - Frequency Domain Measurements: TRL Calibration

Using the TRL calibration method, the rectified vector network analyzer transmission measurements for the pass-through type and stub type plated through hole via structure are shown in Figures 10 – 11.

Figure 8 – S21, Pass Through Plated Through Hole Via, TRL Calibration
Figure 9 – S21, Stub Type Plated Through Hole Via, TRL Calibration

The measurement clearly illustrates the two trends seen in the SOLT calibrated frequency domain measurement. The stub type plated through hole via structure is resonant at 15.5GHz and the pass-through type via structure is relatively well behaved over the measured bandwidth with little deviation from a transmission line.

When compared to the SOLT calibrated data, the most significant difference is the change in the level of loss for the structures being tested. The TRL calibrated data has much less attenuation over the measured bandwidth and with respect to the resonant stub type plated through hole via structure, the TRL calibrated data has a much sharper Q factor. It appears that the low pass filtering effects of the SMA signal launch and the stripline transmission line structure influence the measured data.
The TRL calibrated $S_{11}$ frequency domain data for the pass-through and stub type plated through hole via structures is seen in Figures 10-11.

Figure 10 – S11, Pass Through Plated Through Hole Via, TRL Calibration
Figure 11 – S11, Stub Type Plated Through Hole Via, TRL Calibration

The reflection measurements of the TRL calibrated plated through hole structures have responses similar to the SOLT calibrated data taken for the same structure. The interesting experimental nature of this study is illustrated when the SOLT calibrated reflection terms are plotted against the TRL calibrated reflection terms for the pass-through plated through hole via case as shown in Figure 12.
Figure 12 – S11, SOLT vs TRL Calibration Method

The TRL calibrated measurement shows a small amount of the high frequency combing seen in the SOLT calibrated measurement. However, the combing between the two distinct calibration types is not in phase. This implies that in the case of the pass through plated through hole via structure, where the impedance of the via is relatively well-matched to the characteristic impedance of the printed circuit board, that the reference plane is shifted with the error correction. However, there are still artifacts from the SMA/cable interface reflecting with respect to the front end of the instrument. This potential error source is an important finding with respect to the TRL in-fixture calibration method and applications where it may be used in the future.
3.3 - Time Domain Measurements

Figure 13 shows the time domain reflection profile for the pass-through plated through hole via structure.

![Time Domain Reflection Profile](image)

**Figure 13 - TDR of Pass Through Plated Through Hole Via Structure**

The reflection profile shows a characteristic impedance of the fixture between forty-seven and fifty-three ohms. The first discontinuity seen at approximately 0.35ns is the mismatch created by the SMA and test cable attachment. The first stripline transmission line (from the TDR driven end) in the printed circuit board runs from approximately 0.5ns to 1.0ns. This signal trace has a peak impedance of approximately fifty-one ohms. The pass-through plated through hole via structure is shown at approximately 1.1ns and has a measured impedance of 47Ω. The reflection profile for the stub type plated through hole via structure is shown in Figure 14.
Figure 14 – TDR of Stub Type Plated Through Hole Via Structure

The measured impedance of the stub type plated through hole via test structure is 43Ω compared to the defined characteristic impedance of 50Ω.

The time domain reflection profiles of both the pass-through type and stub type plated through hole via structure illustrate that the printed circuit board test fixtures were fabricated with a 10% impedance tolerance for the stripline transmission lines. The measurements also illustrate that both plated through hole via structures have a lower impedance than the fifty ohm characteristic impedance of the printed circuit board. In time domain reflectometry, impedances that are higher than the characteristic impedance of the system have been determined to be inductive discontinuities. Conversely, impedances that are lower than the characteristic impedance of the system have been determined to be capacitive in nature [Hew98]. In this series of measurements,
both the pass-through plated through hole via structure and the stub type plated through hole via structure have been determined to be capacitive from their reflection profiles with the stub type plated through hole via having the largest reflection coefficient. The stub type via also exhibited a ringing in the reflection profile seen after the impedance drop created by the structure under test in contrast to the pass-through style plated through hole via.
CHAPTER 4

FULL WAVE SIMULATION

Chapter 4 describes the full-wave simulation technique as applied to plated through hole via structures. It details the type of simulation tool used in the analysis, techniques which must be applied when using this tool, the limitations of the full-wave tool, and also decomposes the plated through hole via structures into linear elements to highlight their coupling effects on via structures.

4.1 - Full-Wave Simulation Tool

A commercial electromagnetic simulation package was used to simulate plated through hole via structures in this study. The full-wave simulation tool makes use of the finite integration technique. Finite Integration Technique (FIT) "is a discretization method which transforms Maxwell’s equations onto a dual grid cell complex, resulting in a set of discrete matrix equations. The degrees of freedom collected in the vectors of this discretization scheme, typically consist in physically measurable, integral quantities such as voltages, currents or charges.” [Sch96] The FIT approach to modeling three dimensional electromagnetic structures is unique in that it solves the integral form of Maxwell’s equations and physical quantities to simulate the electromagnetic response of a structure to an input source. The simulated outputs of the full-wave tool are the frequency domain scattering parameters and the time domain response to an impulse. In the time domain comparison, the impulse response of the full-wave tool is
integrated later to determine the step response used by the time domain reflectometer. These simulated results are compared with experimental results.

4.2 - Simulation Strategy And Techniques

The full-wave modeling tool used in this series of simulations solves Maxwell's equations in the modeling space using voltages, currents, etc. Therefore, the method of discretizing the space is a critical factor when evaluating the output of the simulation. In practice, the discretization of the simulation space is referred to as meshing. If the structure is not meshed properly, the simulation will provide non-physical results. This is avoided by limiting the largest mesh element in the full-wave model to a size of no greater than a tenth of one wavelength.

The plated through hole via test structure used in this series of experiments is part of a printed circuit board, which is composed of laminated, alternating conductive planes and dielectric layers (see section 2.1). These conductive planes are very thin, on the order of 30 microns, while the dielectric structure can be an order of magnitude thicker than the conductive layer. This aspect ratio causes the plated through hole via test structure to be difficult to mesh appropriately without consuming significant computational resources. This aspect ratio issue is an important consideration when creating the three dimensional full-wave models and is an important factor in the decision to begin
modeling basic structures before trying to understand the entire complicated plated through hole via structure.

Plated through vias have pads, barrels, anti-pads, and dielectric layers. Each of these elements determines the frequency dependent loading seen in the measurements of Sections 3.1 through 3.3. An interesting approach to understand via structures more accurately would be to apply the principal of superposition. Since all of the structures that are grouped together to form a plated through hole via structure exhibit linear characteristics, this approach simplifies our understanding of these structures. Starting with a basic stripline in a dielectric layer with grounded planes above and below, the model will be created by adding layers, signal pads, anti-pads, and center conducting barrels. The influence of each of the components on the plated through hole via structure will be clear and the results will be built on known good meshing structures.

4.3 - Stripline Structure

As a baseline, the entire printed circuit board was not modeled. Using a more simplistic approach, a full-wave model representing the fifty ohm characteristic impedance stripline transmission line shown in Figure 15 was created.
The time domain results from the baseline model are shown in Figure 16.

Unfortunately, the results from the basic stripline model do not reflect the desired 50 Ohm characteristic impedance as measured in the test fixture. If the model for the stripline structure on layer 3 can not be accurately modeled, it is not relevant to model the entire plated through hole test via structure.
In this initial model, there are two areas with poor impedance match which need to be addressed before moving forward with the full-wave analysis. The first is the discrete port element which launches a signal from a perfect electrical boundary condition onto the stripline transmission line. The simulated impedance measurement of the discrete port was initially as low as 47 Ohms. The second area of concern is the 43.5Ω characteristic impedance of the stripline simulation. In order to improve the impedance of these two areas, the discretization of the modeled structure itself must be taken into consideration.

An area of modeling that often proves difficult for less sophisticated users of three dimensional electromagnetic modeling tools is knowing whether the visual object is properly discretized. The object in the three dimensional model is not always represented properly by the simulation tool's discretization algorithm. In the case of the stripline transmission line structure, the recommended discretization of conducting planes is at least one mesh element thick to properly reflect their spatial location. To improve the quality of the baseline simulation, the stripline conductor was re-meshed with a larger number of elements. As the number of elements used to represent both the width and length of the stripline conductor is increased, the characteristic impedance of the baseline model becomes closer to the desired characteristic impedance of 50Ω. To derive the desired impedance using the simulation tool, a slight change in the width of the conductor was also required. This deviation in width from nominal values can be attributed to the chemical etching process in the manufacturing of printed circuit
boards. The amount of time that a conductor is left in the etching solution determines the amount of copper left in an area of the printed circuit board's layers. Etch solution time can vary from printed circuit board to printed circuit board, and conductor widths may vary with a +/- 5% tolerance. The resulting impedance of the stripline structure is shown in Figure 17.

![Figure 17 - TDR of Re-Meshed Full-Wave Stripline Structure](image)

The second concern in modeling the stripline transmission line is the discrete port elements used to launch a signal into the three dimensional structure. These discrete ports have two areas of freedom, the impedance and the length. The measurements used in this study are based in a 50Ω characteristic impedance environment, and to reduce the number of post-processing steps, the simulation environment should adhere to the same characteristic impedance. This determines the characteristic impedance of the discrete port to be 50Ω.
throughout the bandwidth of the model. The critical variable which influences the impedance of the discrete port is the length. The length of the discrete port determines the inductance and resistance associated with the elements used to represent the port in the modeling tool. The length of the discrete port also influences the capacitance between the end of the stripline trace and the perfectly conducting electrical boundary used as a reference for the discrete port. If the discrete port used is too short, the capacitance between the end of the stripline and the boundary dominate the impedance of the port; if the discrete port is too long, the inductance associated with the port is more significant in influencing the impedance of the structure. To determine a reasonable length for the excitation, a series of experiments which varied the length of the discrete port were established. Using the baseline model as a starting point, additional models were created with differing port lengths. Initially, the discrete port was made to be 0.001 in. long, this length was found to have an impedance significantly lower than the desired 50Ω impedance. In the second round of experiments, the length of the port was increased from 0.001 in to 0.002 in; this change in length increased the impedance of the discrete port element. However, this port length was still lower in impedance than the 50Ω characteristic impedance of the stripline trace. After additional simulation trials, the return loss and time domain reflection profiles for each of the simulations were determined. The discrete excitation element which illustrated the lowest return loss characteristics and closest match to the desired 50Ω impedance was used in this
analysis. The optimal port length for this series of experiments was found to be 0.003 inches. In an FR-4 dielectric, this length corresponds to 0.007 of a wavelength at 20 GHz and correspondingly, will not influence the simulated data.

4.4 - Stripline Structure in Representative Printed Circuit Board Stack-Up

The stripline structure evaluated in section 4.3 was incorporated into a simulation including the remaining layers of the printed circuit board structure used in this series of experiments as shown in Figure 18.

Figure 18 – Full-Wave Model of Stripline Structure in Test Fixture

The results from this simulation are shown in Figure 19.
The characteristic impedance of the stripline structure itself increased with the addition of the remaining layers of the printed circuit board. In this new simulation, which includes additional layers, the discretized representation of the stripline transmission line and all associated reference planes are identical to those of the improved, simpler version of the baseline model. As the size of the model itself became larger, the number of mesh elements in the simulation space increased. This increase in mesh elements (or simulation size) have influenced the impedance of the stripline structure. This variation is small and is within the manufacturing tolerances of the printed circuit boards used in this study, but it should be evaluated in future work.

**Figure 19 – TDR of Stripline Structure in Test Fixture**

![Figure 19 – TDR of Stripline Structure in Test Fixture](image)
4.5 - Stripline Structure in Printed Circuit Board With Signal Pad

As shown in Figure 20, plated through hole via structures have cylindrical pads which anchor them to the printed circuit board and connect them to signal traces in the printed circuit board. These pads typically have a diameter of 0.012in greater than the drill size used to create the plated through hole via. It is important to understand the affects of these pads on via structures because there are a minimum of three pads on any plated through hole structure, one at each end and one at the signal connection.

Figure 20 - Stripline Structure With Pads Added

Figure 21 shows that there is a significant change in the impedance of a stripline structure. By adding a single signal pad to the stripline structure, in the printed circuit board, the impedance of the structure was decreased by more than 5Ωs.
Figure 21 – TDR of Stripline Structure With Pads Added

The capacitive decrease in impedance is associated with the increased width of the stripline where the pad has been added. The effects of the signal pad can be compensated for in a printed circuit board with an anti-pad or clearance in the ground plane below the structure.

4.6 - Printed Circuit Board With Stripline Trace and Anti-Pad

Anti-pads in printed circuit boards are the clearances required by inner conductive ground layers so that the plated through hole via structure signals do not short to ground. The values used for anti-pad clearances vary because of their affect on impedance. Minimal diameter values typically used are 0.024in greater than the diameter of the drill size used to define the plated through hole via structure. Figure 22 represents the full-wave model used, including the
stripline transmission line and the anti-pads used in the plated through hole via structure study.

Figure 22 – Stripline Structure With Anti-Pads

The results from the simulated stripline structure with the anti-pad are shown in Figure 23. The change in impedance from that of the stripline transmission line alone is significant. At approximately 250ps (anti-pad location in the grounded reference planes in the simulation), the impedance of the stripline trace increases to an impedance of approximately 60 Ohms. This inductive discontinuity is indicative of a discontinuity created by a loss of signal return path. Slotted ground planes in printed circuit boards with adjacent stripline transmission lines also present this type of behavior.
Figure 23 – TDR of Stripline Structure With Anti-Pads

4.7 - Plated Through Hole Via Structure Full-Wave Model

Using the nominal printed circuit board layer detail, a model representing the resonant stub type of plated through hole via and non-resonant pass-through type plated through hole via were created in the full-wave simulation tool. All of the plated through hole vias, pads, anti-pads, and stripline traces were included. The models also incorporated the 12700 microns of stripline used to represent post TRL calibrated frequency domain measurements. In the three dimensional modeling tool, all conductors were assigned the material properties of copper and the printed circuit board dielectrics were assigned material values associated with FR-4 epoxy. The surface plating of the outer-most layers of the printed circuit board was neglected because of the necessary simulation resources.
required to properly reflect the resistive effects of a layer of material less than 20 microns thick. Subsequently, the FR-4 epoxy glass layers are represented as solid dielectric blocks rather than the woven structure typically seen in printed circuit boards. Simulation constraints, which can be related to the number of mesh elements and model runtime, influenced the modeling of ground layers and the stripline trace itself. The optimum modeled thickness for these structures, using the available computational resources, was two mesh elements thick with the dielectric layers being at least eight mesh elements thick, as found for the stripline simulation in Section 4.4. In this series of experiments, the energy level within the simulation was set to -50dB. Therefore, the simulation ended when the energy existing in the model, after the excitation, was less than -50dB.

The full-wave model frequency domain and time domain results for the pass-through plated through hole via structure and the stub type plated through hole via structure are given as scattering parameters shown in Figures 24 – Figures 29.
Figure 24 – S11, Pass Through Via, Full-Wave Modeling

Figure 25 – S21, Pass Through Via, Full-Wave Modeling
Figure 26 – TDR, Pass Through Via, Full-Wave Modeling

Figure 27 – S11, Stub Type Via, Full-Wave Modeling
Figure 28 – S21, Stub Type Via, Modeling

Figure 29 – TDR, Stub Type Via, Full-Wave Modeling
The frequency domain results were similar to the measured data taken in Section 3.3. The simulation of the stub type plated through hole via structure showed a strong resonance at 15.5GHz and also exhibited increased reflections in that same bandwidth of interest. The time domain reflection profile for the resonant stub case simulation has an impedance of 41.5 Ohms. The pass-through plated through hole via structure has a smooth transmission characteristic, as compared to the resonant structure, and it had significantly lower levels of reflections. The impedance as simulated yielded an impedance of 51 Ohms.
CHAPTER 5

THREE DIMENSIONAL QUASI-STATIC SIMULATION

Chapter 5 describes the quasi-static simulation of plated through hole via structures and the techniques used to derive an equivalent circuit representation of the via structures investigated in this study. The chapter highlights the tool used, the output of the simulation tool, the limitation of quasi-static analysis, and how the coupling terms detailed in Chapter 4 apply to the equivalent circuit representation of a plated through hole via structure.

5.1 - Quasi-Static Simulation Tool

Quasi-Static simulations are different from the full-wave electromagnetic simulation tools used in Chapter 4. The full-wave simulator used in this study solves an integral form of Maxwell’s equations in a discretized space. Electromagnetic field solvers that employ this technique contain information about the electric and magnetic fields, and preserve the coupled relationship between the two fields. Conversely, quasi-static simulations, by ignoring the displacement current term in Maxwell’s equations, do not maintain the relationship between the electric and magnetic fields. Quasi-static simulations are characterized by the decoupling of the electric and magnetic fields, which allows the two quantities to be solved independently in the solver.

An example of how quasi-static simulation tools neglect displacement current is highlighted in investigations into the flow of current in conductors. At DC the distribution of current in the conductor is uniform. As frequencies
increase, the distribution of charge within the conductor changes. This change in
current is referred to as the displacement current. When the displacement
current term is neglected, the electric fields outside of the conductor remain
constant as the currents change inside the conductor. This constraint makes
quasi-static field solvers inaccurate at describing structures whose size is smaller
than an eighth of one wavelength at a given frequency.

The output of a quasi-static electromagnetic field solver is the resistance
and inductance terms associated with the magnetic field, and the capacitance
and admittance terms associated with the electric field. These quantities can
then be used to determine networks that represent the structures under test and
can be incorporated into a circuit simulation tool such as SPICE.

The quasi-static simulation tool used in this study is based on the finite
element electromagnetic modeling technique. Three dimensional modeled
structures are divided into a mesh composed of finite elements. In the quasi-
static three dimensional solver, a tetrahedron style mesh is used to break the
modeled structure into elements. After the mesh is established, the quasi-static
field solver computes the electromagnetic field pattern inside the structure
[Ans06]. The field pattern is then evaluated and re-meshed with an increased
number of tetrahedrons in the areas of highest energy concentration. After the
initial simulation, the tool re-computes the electromagnetic field pattern and
compares the result to the previous iteration until the net change in the field
values is within a user-specified input parameter. Once the simulation
termination criterion is met, the resistance, inductance, admittance, and capacitance values are extracted from the field quantities.

The output of the quasi-static simulation tool used in this study is a Maxwellian Capacitance Matrix and a partial Inductance Matrix. Maxwellian Capacitance Matrices illustrate the relationship between charge and voltage on a defined number of conductors given a known boundary condition in the simulation. For example, in a simulation model of four conductors, the Maxwellian Capacitance Matrix will have the following form:

\[
\begin{bmatrix}
Q_1 \\
Q_2 \\
Q_3 \\
Q_4 \\
\end{bmatrix} =
\begin{bmatrix}
C_{11} & C_{12} & C_{13} & C_{14} \\
C_{21} & C_{22} & C_{23} & C_{24} \\
C_{31} & C_{32} & C_{33} & C_{34} \\
C_{41} & C_{42} & C_{43} & C_{44} \\
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2 \\
V_3 \\
V_4 \\
\end{bmatrix}
\]

Figure 30 – Maxwellian Capacitance Matrix

where \( Q \) is the charge matrix, \( C \) is the capacitance matrix, and \( V \) is the voltage matrix. With a known potential on a conductor and with all other conductors in the system grounded, the capacitance between the conductor and another conductor in the model can be determined by the amount of charge on that conductor. An inductance matrix describes the relationship between flux linkage and current flow (or voltage changes and time varying currents) [Ans06] around a closed loop circuit path. A partial inductance matrix is similar to an Inductance matrix with the exception that the inductance is measured for an open circuit path rather than a closed circuit path. Terminals are assigned to various points along the current path and the current density between those terminals
determines the partial inductance. This implies that the partial inductance matrix accounts for a part of a current path to account for the total current path around a circuit loop, the partial and self inductances for each piece of the closed current path must be added.

5.2 - Quasi-Static Tool Techniques and Evaluation

Electromagnetic simulation tools provide output parameters which are dependent on boundary conditions, excitation methods, and other user-defined inputs. These input parameters determine the validity of data derived from simulation. Because of their geometric complexity, plated through hole vias require computational tools to be analyzed and are not easily expressed through analytical methods. To build confidence in the simulation methodology, an analysis of general structures that have closed form solutions is performed. A coaxial transmission line structure is used to identify weaknesses of the quasi-static electromagnetic field solver.

Coaxial transmission lines are composed of a circular center conductor and a conducting outer shield surrounding the center conductor as shown in Figure 31.
The capacitance per unit length of the coaxial transmission line is derived in Appendix E and is as follows:

\[
C/\ell = \frac{2\pi e}{\ln \left( \frac{b}{a} \right)} \quad \text{[Farads/meter]}
\]  

(5-1)

The inductance of the coaxial transmission line per unit length is derived in Appendix E:

\[
L/\ell = \frac{\mu}{2\pi} \ln \left( \frac{b}{a} \right) \quad \text{[Henries/meter]}
\]  

(5-2)

In the quasi-static electromagnetic simulation tool, two coaxial transmission lines were drawn with lengths of 3mm and 1mm. The difference between the two lengths of transmission line removes any interaction between the ends of the structure and the boundary in the simulation space. The radius from the center conductor to the outer ground shield is 1.48mm (a) and the radius of the center conductor itself is 0.406mm (b). The simulated capacitance and inductance for the 3mm model were determined to be 0.16608pF and 0.67458nH. The simulated capacitance and inductance for the 1mm case was
determined to be 0.078991pF and 0.1183nH. The difference in capacitance for the two simulations was found to be 0.0871pF, and the difference in inductance for the two simulations was found to be 0.5562nH. However, these values are associated with a piece of coaxial transmission line that is 2mm in length. When the inductance and capacitance values are reduced to per unit length form, the capacitance was found to be 4.35e-11F/m and the inductance was found to be 2.781e-7H/m. From the closed form equations listed earlier, the capacitance per unit length was found to be 4.2992e-11F/m and the inductance per unit length was found to be 2.5867e-7H/m. The experimental error for the capacitance per unit length is 0.5%, while the experimental error for the inductance per unit length is 3.6%.

Agreement between the closed form solution and the quasi-static field solver for the case of a coaxial transmission line establishes that the simulation can produce correct values and that the user techniques being applied are reasonable. The same modeling process can now be applied to the case of a plated through hole via structure to determine the lumped capacitance and inductance associated with the structure.
5.3 - Equivalent Circuit Representation of Via Structures

As described in Section 4.2, plated through hole vias are complicated structures which can be considered as the combination of simpler linear structures. In Sections 4.4-4.6, plated through vias were evaluated in a full-wave electromagnetic field solver to illustrate the influence of the stripline connections, pads, and anti-pads on via structures. Since all of the aforementioned via components are linear and superposition applies to the structure, the coupling terms can be used to create a lumped element representation of the structure.

From the evaluation performed in Sections 4.4-4.6, it was determined that signal pads attached to a basic stripline structure produced a capacitive decrease the impedance and the relief placed in the ground planes of printed circuit boards (anti-pads) produced an inductive increase in impedance. Stub portions of plated through hole via structures produced a decrease in impedance. It has been previously shown that right angle connections between stripline structures and plated through hole via structures produces a decrease in impedance.

The first plated through hole via structure represented is a pass-through type via structure. Section 2.1 describe the physical pass-through via structure being evaluated in this study. The pass-through via includes two right angle stripline connections, one on layer three and another on layer six. These stripline to plated through hole via connections create a short unused portion of the plated through hole via between layers one and three, and between layers six and eight.
The pass-through via also includes a long portion of the plated through hole which functions as a transmission line transitioning between the two signal layers. One proposed lumped element representation of this structure is a basic 'PI' network model illustrated in Figure 32.

![Figure 32 - 'PI' Network Representation](image)

In this 'PI' model, the two capacitors at each end represent the capacitive discontinuity seen in stubs. This discontinuity is caused by two factors: the right angle transition from stripline to plated through hole via, and the fringing fields associated with the ends of the plated through hole via barrel. The inductance represents the long barrel portion of the plated through hole used as a transmission line. Future work for this study could include adding some resistance in parallel with the inductance to represent the losses associated with plated copper printed circuit board structures.

The second plated through hole via structure that is addressed is the stub type plated through hole via. The stub type via structure was determined to be the most difficult structure to evaluate in the quasi-static electromagnetic field solver because of the current return path. This will be described in more detail in section 5.4. The stub type plated through hole via structure as described in
section 2.1 contains a continuous stripline transmission line structure on signal layer three and a shunt, stub element from layer three to layer eight. A representation of this shunt element could be a capacitor. While a capacitor will not create the highly resonant nature of stub type vias seen in section 3.3, it does represent the strong negative change in impedance from a baseline transmission line structure. Future work on the development of this model should include the inductances associated with the shunt element and the inductances/resistances seen as the transmission line structure passes over the clearance in the ground planes for the signal connections. Determining these inductances will prove to be difficult for the quasi-static simulation tool used in this study, because of the return path definition.

5.4 - Quasi-Static Plated Through Hole Via Models

Two models for the inductance and capacitance of the pass-through type plated through hole via structure were created. To determine the capacitance of the pass-through type via structure, a model was created of a piece of stripline transmission line on signal layer three equivalent to the total length of stripline used in the simulations. This stripline structure did not pass over any clearances in the ground plane and was a uniform structure throughout the model. The second model created to determine the capacitance of the pass-through plated through hole via structure included the stripline on both layers three and six, the plated through hole itself, and all other attachments to the plated through hole
via. From the principal of superposition, the difference in capacitance between these two models determines the capacitance of the plated through hole via structure itself. The difference in capacitance between the two simulations was determined to be 0.435pF. The inductance of the pass-through plated through hole via structure was found in a similar manner. To determine the inductance of the via structure, the return path of the current needs to be addressed. The returning current in a plated through hole via use the adjacent ground vias and the grounded planes to form a return path. Two models were created to isolate the return path of the current. The first model included the entire plated through hole structure until it reached layer four (ground) where the via structure was shorted out. The second model shorted out the plated through hole via at layer seven. Shorting the via structure forces the current to use the true ground path of the modeled structure (ground vias, and ground planes); this is one method of using a partial inductance solver to determine complete current paths. The change in inductance between the two simulations is the inductance associated with the plated through hole via structure. The change in inductance between the two simulations for the pass-through plated through hole via structure model was determined to be 0.5254nH.

The capacitance and inductance values are then placed into a ‘PI’ network representation. Exactly one half of the capacitance was used on each end of the ‘PI’ network, and the full inductance value was used in the network’s inductive element. The completed model was then incorporated into a SPICE simulation.
tool for frequency domain evaluation. The SPICE model also incorporates the losses associated with the stripline transmission line attached to the via structure. These losses are not part of this study, but are relevant for the correlation work in Section 6. Figures 33 - 34 describe the results of the simulations.

Figure 33 – S11, Pass Through Via, Equivalent Circuit Model
The equivalent circuit model used in SPICE illustrates smooth transmission characteristics throughout the frequency bandwidth of interest and also illustrates a reflection response characteristic of a piece of transmission line with a discontinuity at each end.

Two models of the inductance and capacitance for the stub type plated through hole via structure were also created. The capacitance term was determined through a similar approach to the pass-through style plated through hole via model. Two simulations were created, one having uniform stripline and the other having the stripline with the plated through hole via structure. The change in capacitance between the two models was found to be 0.44392pF.

The inductance for this simulation could not be determined in a manner similar to the pass-through via case. The stub portion of the plated through hole
via structure carries current, but the quasi-static method of determining that returning current is difficult. There is not a physically based method of shorting the plated through hole via structure to force the return currents through the ground system because the stub type via is not in the path of the energy as in a pass-through type via; it is more of a shunt element.

A lumped element representation of the stub type plated through hole via structure was created in SPICE. Similar to the pass-through plated through hole via model described earlier, the model includes the necessary losses from the FR-4 dielectric. The frequency domain results from the SPICE simulation are shown in Figures 35-36.

![S11: Pass-Through Plated Through Hole Via Structure, Equivalent Circuit Model](Figure 35 - S11, Stub Type Via, Equivalent Circuit Model)
As section 5.3 predicted, the capacitive representation of the stub type plated through hole via structure did not predict the highly resonant nature of the stub via structure and illustrated relatively smooth transmission through the bandwidth of interest.
CHAPTER VI is a comparison of quasi-static and full-wave models. The scattering parameters resulting from quasi-static equivalent circuit model, a full-wave model, and measurements, as applied to two types of plated through hole via structure, are evaluated. Weaknesses of each of the simulation techniques are highlighted, as well as measurement inaccuracy.

6.1 - Stub Type Plated Through Hole Via Structure Analysis

The results from this study illustrate the strengths and weaknesses of two simulation methodologies, as well as the measurement techniques applied. The frequency domain data from sections 3, 4, and 5 were combined and plotted together to illustrate the differences in techniques for the stub type plated through hole via structure. Because of its interesting behavior, the stub type plated through hole via analysis was performed first. The frequency domain results from the stub via analysis are shown in Figures 37-38.
Figure 37 – S21, Stub Type Via Comparison

Figure 38 – S11, Stub Type Via Comparison
In the transmission data, the full-wave model showed strong correlation with the TRL de-embedded measurement. The resonant notch frequency was predicted within 700 MHz of the measured value by the full-wave model. There is a delta in the resonant frequency predicted by the quasi-static simulation, the full-wave simulation and the measurement. As discussed in Section 5.3, the equivalent circuit representation of the stub type via could not predict resonant behaviors for frequencies greater than an eighth of the simulated structures wavelength. The deviation between the resonant frequencies of the full-wave model and the measurement is related to the tolerances associated with manufacturing printed circuit boards. The full-wave model created was based on the nominal values of the printed circuit board used in this study, whereas the printed circuit board itself is subject to variations associated with the dielectrics used in separating the various layers. These variations affect not only the electrical properties associated with the dielectric, but also the mechanical properties associated with the material. As an example, if the length of the stub was decreased by 10% of the board thickness, the result would be as shown in Figure 39 and the new resonant frequency associated with the stub via has moved ahead of the initial modeled value by 1.1GHz.
The reflection terms for the full-wave simulation and those of the measurements also showed strong correlation above 1 GHz. The measurements exhibited combing that was not in the simulated data. It may be attributed to the on-board TRL calibration method applied to the test fixture. The frequency of the combing relates to the length of stripline trace between the SMA jacks on the test fixture without any de-embedding techniques applied. The lumped element model correlated well with the measurements up to a frequency of 7 GHz, at which point, the resonances of the stub via become significant. At frequencies equivalent to or less than one eighth of a wavelength, this approach to modeling did not correlate with measurement. As expected, the capacitive element lacked the strong resonance exhibited by the stub via structure. In the time domain, the
TDR of the full wave model predicted an impedance of 41.6 Ohms at resonance as shown in Figure 40.

![Figure 40 - TDR, Stub Type Via Full-Wave Model](image)

This impedance is the change between the characteristic impedance of the stripline trace in the modeled structure and the impedance of the via. In the full wave simulation, this change is 9.8 Ohms. A time domain transform of the TRL de-embedded frequency domain data was completed using a commercially available software package. The transform indicated a lower impedance of 42 Ohms, which corresponds to the change in the full wave model. The deviation between the TDR of the full wave model and the direct measurement is attributed to the additional stripline etch in the printed circuit board and to the high frequency filtering effects of the SMA cable attachment, which were both included in the direct measurement.
6.2 - Pass-Through Plated Through Hole Via Analysis and Comparison

As in section 6.1, the frequency domain data from sections 3, 4, and 5 were combined and plotted together to illustrate the differences in simulation technique for the pass-through type plated through hole via structure. Figure 41 illustrates the transmission correlation for the pass-through via study. The models and measurement are in agreement up to 16GHz, which is less than one eighth of a wavelength for the equivalent circuit model. The full-wave model and measured data continue to agree to the 20GHz limit.

![Figure 41 - S21, Pass Through Via Comparison](image)

In Figure 42, the reflection terms for the non-resonant via case are shown. Both of the simulated methods did not illustrate any relationship to the measured data at frequencies below 15 GHz. The reflective nature of the lumped element model
predicted the highest level of reflection, while the full-wave simulation showed the lowest level of reflection, and the measured data fit between the two simulated responses.

**Figure 42 - S11, Pass Through Via Comparison**

In a TDR plot of the full-wave model, shown in Figure 43, the data illustrate a very well-matched via structure. It is difficult to compare because of the noise level in the network analyzer. The deviation of the impedance for the entire model is less than 1.5 Ohms from the characteristic impedance of stripline trace. The TDR directly measured in Figure 44 illustrates an impedance of 48.4 Ohms, and correspondingly, a deviation of 2.5 Ohms in the impedance of the plated through hole via from that of the stripline trace. Applying the time domain transform used in the resonant via analysis, an impedance deviation of 4 Ohms was measured. As the impedance match of the via structure under test
improved, the reflections decreased, and correspondingly, the accuracy of the modeling methods became difficult to determine against measurements that approached the calibrated receiver levels of the VNA.

Figure 43 - TDR Pass Through Via, Full-Wave Model
Figure 44 - TDR, Pass Through Via Measured
Chapter 7 is a review of Chapters 1-6 and stresses the results section through tabulated data points detailing the differences between full-wave simulation, quasi-static simulation, and measurement. The conclusions presented include recommended bandwidths/signaling rates for the two simulation methods, sources of calibration and measurement error, and design opportunities for future studies.

**7.1 - Simulation Methodologies**

In modeling plated through hole via structures (or any three dimensional structure), it is essential to determine the required bandwidth and end application of the simulation. In this analysis, two distinctly different electromagnetic approaches were taken to simulate a plated through hole via structure, quasi-static and full-wave. The quasi-static approach taken made use of the principle of superposition and is therefore dependent on the linear nature of via structures. In contrast, the full-wave simulation method applies Maxwell’s Equations to a discretized simulation space. Tables 1 and 2 compare the simulations with measured data for two different plated through hole via structures.
### Table 1: Stub Type Plated Through Hole Via Results

<table>
<thead>
<tr>
<th>Freq (GHz)</th>
<th>Measured (dB)</th>
<th>Full-Wave (dB)</th>
<th>Equivalent Circuit (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>-0.086</td>
<td>-0.055</td>
<td>-0.099</td>
</tr>
<tr>
<td>1</td>
<td>-0.146</td>
<td>-0.09</td>
<td>-0.175</td>
</tr>
<tr>
<td>2</td>
<td>-0.251</td>
<td>-0.199</td>
<td>-0.32</td>
</tr>
<tr>
<td>3</td>
<td>-0.394</td>
<td>-0.334</td>
<td>-0.469</td>
</tr>
<tr>
<td>4</td>
<td>-0.519</td>
<td>-0.505</td>
<td>-0.633</td>
</tr>
<tr>
<td>5</td>
<td>-0.634</td>
<td>-0.68</td>
<td>-0.798</td>
</tr>
<tr>
<td>6</td>
<td>-0.817</td>
<td>-0.84</td>
<td>-0.943</td>
</tr>
<tr>
<td>7</td>
<td>-0.981</td>
<td>-1.058</td>
<td>-1.075</td>
</tr>
<tr>
<td>9</td>
<td>-1.625</td>
<td>-1.764</td>
<td>-1.365</td>
</tr>
<tr>
<td>10</td>
<td>-1.886</td>
<td>-2.232</td>
<td>-1.493</td>
</tr>
<tr>
<td>12</td>
<td>-3.311</td>
<td>-3.882</td>
<td>-1.644</td>
</tr>
<tr>
<td>15</td>
<td>-10.99</td>
<td>-16.36</td>
<td>-1.908</td>
</tr>
<tr>
<td>17</td>
<td>-8.911</td>
<td>-7.29</td>
<td>-2.238</td>
</tr>
<tr>
<td>19</td>
<td>-5.33</td>
<td>-4.441</td>
<td>-2.938</td>
</tr>
<tr>
<td>20</td>
<td>-4.596</td>
<td>-4.251</td>
<td>-3.455</td>
</tr>
</tbody>
</table>

### Table 2: Pass-Through Type Plated Through Hole Via Results

<table>
<thead>
<tr>
<th>Freq (GHz)</th>
<th>Meas (dB)</th>
<th>Full-Wave (dB)</th>
<th>Equivalent Circuit (dB)</th>
<th>Full-Wave (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>-0.095</td>
<td>-0.007</td>
<td>-0.096</td>
<td>-0.0509</td>
</tr>
<tr>
<td>1</td>
<td>-0.159</td>
<td>-0.021</td>
<td>-0.172</td>
<td>-0.091</td>
</tr>
<tr>
<td>2</td>
<td>-0.266</td>
<td>-0.081</td>
<td>-0.32</td>
<td>-0.161</td>
</tr>
<tr>
<td>3</td>
<td>-0.379</td>
<td>-0.176</td>
<td>-0.469</td>
<td>-0.253</td>
</tr>
<tr>
<td>4</td>
<td>-0.495</td>
<td>-0.293</td>
<td>-0.629</td>
<td>-0.369</td>
</tr>
<tr>
<td>5</td>
<td>-0.599</td>
<td>-0.423</td>
<td>-0.795</td>
<td>-0.489</td>
</tr>
<tr>
<td>6</td>
<td>-0.707</td>
<td>-0.56</td>
<td>-0.94</td>
<td>-0.624</td>
</tr>
<tr>
<td>7</td>
<td>-0.823</td>
<td>-0.701</td>
<td>-1.075</td>
<td>-0.775</td>
</tr>
<tr>
<td>9</td>
<td>-1.116</td>
<td>-0.963</td>
<td>-1.365</td>
<td>-1.102</td>
</tr>
<tr>
<td>10</td>
<td>-1.213</td>
<td>-1.087</td>
<td>-1.493</td>
<td>-1.255</td>
</tr>
<tr>
<td>12</td>
<td>-1.484</td>
<td>-1.333</td>
<td>-1.643</td>
<td>-1.586</td>
</tr>
<tr>
<td>15</td>
<td>-2.13</td>
<td>-1.878</td>
<td>-1.906</td>
<td>-2.33</td>
</tr>
<tr>
<td>17</td>
<td>-3.072</td>
<td>-2.54</td>
<td>-2.239</td>
<td>-3.147</td>
</tr>
<tr>
<td>19</td>
<td>-5.818</td>
<td>-5.846</td>
<td>-2.94</td>
<td>-6.506</td>
</tr>
</tbody>
</table>
In general, Tables 1 and 2 confirm that quasi-static simulation methods do not work well for structures which are smaller than an eighth of one wavelength. However, changes to the equivalent circuit model employed to represent the stub type via structure offer improvements to the quasi-static simulation. As an example, the lumped elements used to represent the stub type plated through hole via structure could include inductance, resistance, and capacitance in a network representation. At frequencies for which the stub is shorter than an eighth of one wavelength, this network could be divided into multiple cascaded networks to represent via structures.

Tables 1 and 2 also illustrate that the full-wave simulation tool performed very well when compared with measurement data and accurately reflected the insertion loss magnitude from 0.1GHz to 20GHz. However, in full-wave simulations, the discretization of the simulation space was determined to be a limitation. As the number of mesh elements increased, the low frequency accuracy of the simulation improved. This is illustrated in Table 7-2 where the low frequency values predicted by a full-wave simulation with 2,695,968 mesh cells are significantly closer to the measured values than the full-wave simulation with 1,122,00 mesh cells. Full-wave models created for this analysis were optimized for simulation on a laptop computer with an Intel Dual-Core 2.33GHz processor and 4 gigabits of random access memory. Improved simulation times, increased computational resources and reductions in cost would allow higher order meshing.
7.2 – Simulation Method Impact on Signaling

In many applications, the desired goal of a simulation is to accurately determine component attributes and then understand their impact on system performance. Telecommunications channels are an example of specific systems using plated through hole via structures in the signal path and are performance metrics for the two simulation methodologies used in this study. The outcome of this channel analysis will be used to distinguish weaknesses of the simulation methods, as well as, identify via structures as critical or non-critical elements in the transmission path.

System analysis utilizes multiple methods to determine the impact of an individual component on the signal path. In this channel analysis, the insertion loss constituent of the scattering parameters is treated as a transfer function which is multiplied, in the frequency domain, by the power spectral density envelope of a digital signal and an RF pulse. Per Rayleigh’s Energy Theorem, the numerical integration of the resultant waveforms determines the total power.

As the demand for bandwidth in the telecommunications industry increases, data rates are approaching ten gigabits per second. The bit period ($T_b$) of a ten gigabit per second binary, Non-Return to Zero (NRZ) digital signal, is $1 \times 10^{-10}$ s which corresponds to a fundamental frequency of 5GHz. The envelope of the Power Spectral Density (PSD) for a ten gigabit per second digital signal is defined as
\[ p(f) = T_b \left( \frac{\sin \pi f T_b}{\pi f T_b} \right)^2 \]

Figures 45 and 46 illustrate the impact of the plated through hole via structure and simulation methodology on a ten gigabit per second PSD.

Figure 45 - Pass Through Via vs PSD
As shown in Figures 45-46, the impact of via insertion loss on the fundamental frequency of a ten gigabit per second, NRZ digital signal is small for pass through and stub type plated through hole via structures. Both plated through hole via structures correlated well with measured values and bandwidth attenuation from 0-10GHz is associated with dielectric/conductor loss mechanisms in the printed circuit board.

Variation between simulation and measurement at the third harmonic of the ten gigabit per second, NRZ digital signal (15GHz) is also detailed in Figures 45-46. The impact of this deviation is reflected in an analysis of signal power shown in Tables 3 and 4. As described in Section 7.1, the low frequency performances of the full-wave and quasi-static simulation are very similar. When
this data is coupled with the low frequency spectral content of the NRZ digital signal, conclusive evidence of an advantage in simulation methodology is not available.

Table 3: Stub Type Via Structure, Digital Signal

<table>
<thead>
<tr>
<th>Method</th>
<th>Power</th>
<th>Experimental Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement</td>
<td>1</td>
<td>N/A</td>
</tr>
<tr>
<td>Quasi-Static Simulation</td>
<td>1.01</td>
<td>1.1%</td>
</tr>
<tr>
<td>Full-Wave Simulation</td>
<td>0.99</td>
<td>0.8%</td>
</tr>
</tbody>
</table>

Table 4: Pass-Through Type Via Structure, Digital Signal

<table>
<thead>
<tr>
<th>Method</th>
<th>Power</th>
<th>Experimental Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement</td>
<td>1</td>
<td>N/A</td>
</tr>
<tr>
<td>Quasi-Static Simulation</td>
<td>0.98</td>
<td>1.7%</td>
</tr>
<tr>
<td>Full-Wave Simulation</td>
<td>0.96</td>
<td>4.4%</td>
</tr>
</tbody>
</table>

To remove the low frequency behavior which governed the data shown in Tables 3 and 4, an RF pulse with a center frequency of 15GHz and a period of 0.2ns was used in place of the NRZ digital signal. This type of analysis is significant as encoding schemes are being applied to digital signals which remove the low frequency content of the signals. The integrated power spectral density results of the RF pulse are shown in Tables 5 and 6. As predicted, in the stub type via analysis, the quasi-static model does not agree with measurement and over estimates the signal power while the full-wave model’s error source is
related to the predicted resonance frequency. Additionally, in the pass-through plated through hole via structure analysis, the quasi-static simulation method over estimates the signal power and showed increased deviation from measurement when compared to the full-wave simulation.

<table>
<thead>
<tr>
<th>Method</th>
<th>Power</th>
<th>Experimental Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement</td>
<td>1</td>
<td>N/A</td>
</tr>
<tr>
<td>Quasi-Static Simulation</td>
<td>2.52</td>
<td>152%</td>
</tr>
<tr>
<td>Full-Wave Simulation</td>
<td>0.86</td>
<td>13%</td>
</tr>
</tbody>
</table>

Table 6: Pass-Through Type Via Structure, RF Pulse

<table>
<thead>
<tr>
<th>Method</th>
<th>Power</th>
<th>Experimental Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement</td>
<td>1</td>
<td>N/A</td>
</tr>
<tr>
<td>Quasi-Static Simulation</td>
<td>1.08</td>
<td>7.6%</td>
</tr>
<tr>
<td>Full-Wave Simulation</td>
<td>0.97</td>
<td>3.4%</td>
</tr>
</tbody>
</table>

7.3 - Measurements and Fixturing

To obtain accurate measurement data, the effects of the test signal connections were de-embedded from the via structures. This de-embedding operation was enabled through the use of properly designed adaptors included in the printed circuit board test vehicle. In this study, the TRL calibration method
offered an improvement in measurement quality over the SOLT calibration described in section 3.2. However, as Figure 13 illustrates, the effects of the reflected energy traveling between two SMA discontinuities has not been completely removed by the TRL calibration method. Via structures which were not matched to the 50Ω characteristic impedance of the printed circuit board test fixtures illustrated improved signal to noise characteristics when compared to well-matched via structures.

The noise level of the calibration method determined the quality of the measurement and was not as significant in measuring highly reflective structures as opposed to well-matched structures. The TRL calibration method could be improved by using more uniform dielectrics in the calibration fixture and insertable printed circuit board standards rather than in-fixture standards.

7.4 - Conclusions

In this study, full-wave and quasi-static modeling approaches were used to evaluate a resonant and non-resonant plated through hole structure against a set of measured data. The quasi-static lumped element models correlated well to measured data at frequencies below 2GHz, but the accuracy decreased as the simulated structure size became less than one eighth of a wavelength. Consequently applications are limited at frequencies above 6GHz. By internally determining the significant attributes of the stripline via structure, the electrostatic
and magnetoquasi-static solver focused meshing elements onto less significant features, which generated non-physical capacitive values. Additionally, the partial inductance method requires a prior understanding of the physical return paths for the current to determine the inductance. Consequently, the use of this technique was limited only to the pass-through via and not to the stub via model, as the later did not have a return path through the lower layers in the printed circuit board. The full-wave models predicted the performance of the resonant plated through hole via structure, as well as the frequency domain transmission of the pass-through plated through hole via and accordingly can be used for frequencies above 2GHz. However, the meshing used to discretize the structure is dependent on frequency so that additional mesh elements are needed at higher frequencies. This imposes a computational resource constraint on the full-wave modeling method. As a final point, the plated through hole via structures used in this study, were found to have minor impact on a ten gigabit per second digital signal.

7.5 - Future Work

In this study, there are many opportunities identified for future work in the examination of plated through hole via structures. The required bandwidth for communications channel models is increasing and propels the need for plated through hole via analysis. Digital signaling rates are increasing from ten to
twenty gigabits per second, and a feasibility assessment of forty gigabits per second needs to be performed.

The data shown in section 6.2 illustrate the need for additional plated through hole via structures to be tested. While well-matched pass through type plated through hole via structures showed potential for communications channels requiring 20GHz of bandwidth, many pass through via structures do not have a impedance which is well-matched to the characteristic impedance of the system. Pass through type plated through hole vias which are not well-matched to the normalized impedance of the system should be addressed. This work should include varying the printed circuit board tolerances and the pad/anti-pad dimensions of the plated through hole via structures.

The artifacts of the test signal connections which appeared in the TRL calibrated measurements highlighted the need for improved calibration techniques. Improvements should be made to include a high quality calibration over a frequency domain bandwidth of 0 GHz to 40 GHz. This bandwidth will be required for data rates approaching forty gigabits per second. To improve the calibration at these frequencies, a new approach will be necessary which is not as dependent on characteristic impedance and delay as TRL calibration, and which uses more of the available reflection information in the test fixture.

The need for improved equivalent circuit models is described. Plated through via structures can be interpreted in many different ways, and each version should be evaluated in the appropriate simulation environment. In
industry, there are multiple commercial tools available for creating SPICE compatible models. These tools derive SPICE compatible models from both simulated and measured scattering parameters. An analysis of the models created by these tools will be important to future plated through hole via structure characterization efforts.

The need for understanding plated through hole via structures and via structures in general is clear. Vias are critical elements in device, package, interposer, and interconnect structures. The characterization of these structures requires improved simulation methodologies, measurement capabilities, and tools to translate between the different environments with increasing accuracy at higher signaling rates.
APPENDIX A

SMA Description

Chapter II presents the simple experimental printed circuit board which utilizes SMA connectors to connect inner printed circuit board layers to test equipment. The mechanical drawings and product specifications are as follows

A.1 – Mechanical Drawing

Figure A.47 - SMA Component Drawing
### ENGINEERING DATA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
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<tbody>
<tr>
<td>Nominal Impedance</td>
<td>50 Ohms</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>dc-27 GHz</td>
</tr>
<tr>
<td>Voltage Rating</td>
<td>Sea Level 335 Vrms</td>
</tr>
<tr>
<td>Temperature Rating</td>
<td>70,000 Feet 85 Vrms</td>
</tr>
<tr>
<td></td>
<td>-65° to +150° C</td>
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</table>

### MECHANICAL

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
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</thead>
<tbody>
<tr>
<td>Material</td>
<td>3.3</td>
</tr>
<tr>
<td>Finish</td>
<td>3.3.1</td>
</tr>
<tr>
<td>Design</td>
<td>3.4</td>
</tr>
<tr>
<td>Recommended Mating Torque</td>
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</tr>
<tr>
<td>Force to Engage and Disengage</td>
<td>N/A</td>
</tr>
<tr>
<td>Coupling Nut Retention Force</td>
<td>2 in#</td>
</tr>
<tr>
<td>Coupling Proof Torque</td>
<td>N/A</td>
</tr>
<tr>
<td>Mating Characteristics</td>
<td>N/A</td>
</tr>
<tr>
<td>Connector Durability</td>
<td>500 Cycles</td>
</tr>
<tr>
<td>Center Contact Retention</td>
<td>N/A</td>
</tr>
<tr>
<td>Cable Retention</td>
<td>N/A</td>
</tr>
<tr>
<td>Hermetic Seal</td>
<td>N/A</td>
</tr>
</tbody>
</table>

### ELECTRICAL

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insulation Resistance</td>
<td>5000 Megohms</td>
</tr>
<tr>
<td>Dielectric Withstanding Voltage</td>
<td>650 Vrms</td>
</tr>
<tr>
<td>RF High Potential Withstanding</td>
<td>433 Vrms @ 5 MHz</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>3 Millionths</td>
</tr>
<tr>
<td>Voltage Standing Wave Ratio</td>
<td>1.05 + .0045f(GHz)</td>
</tr>
<tr>
<td>RF Leakage</td>
<td>&lt;(120-fGHz) dB</td>
</tr>
<tr>
<td>RF Insertion Loss</td>
<td>.93-f(GHz)</td>
</tr>
</tbody>
</table>

### ENVIRONMENTAL

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vibration</td>
<td>MIL-STD-202, Method 204</td>
</tr>
<tr>
<td>Shock</td>
<td>Test Condition D</td>
</tr>
<tr>
<td>Thermal Shock</td>
<td>MIL-STD-202, Method 213</td>
</tr>
<tr>
<td>Corrosion(Salt Spray)</td>
<td>Test Condition I</td>
</tr>
<tr>
<td>Moisture Resistance</td>
<td>MIL-STD-202, Method 107</td>
</tr>
<tr>
<td>Corona Level</td>
<td>Test Condition B (150° C)</td>
</tr>
<tr>
<td></td>
<td>500 Megohms</td>
</tr>
</tbody>
</table>

Figure A.48 - SMA Product Specification
APPENDIX B

TEST BOARD DESIGN

B.1 – Layer Descriptions

Chapter II presents the printed circuit board used to analyze the experimental plated through hole via structures. The layer by layer description of the printed circuit board used for calibration and testing is as follows

Layer 1 – Calibration Printed Circuit Board

Figure B.49- Top Layer of Calibration PCB

Layers 2, 4, 5, and 7 – Calibration Printed Circuit Board

Figure B.50 - Ground Layers of Calibration PCB
Layer 3 – Calibration Printed Circuit Board

Figure B.51 - Signal Layer 3 Calibration PCB

Layer 6 – Calibration Printed Circuit Board

Figure B.52 - Signal Layer 6 Calibration PCB

Layer 8 – Calibration Printed Circuit Board

Figure B.53 – Layer 8 Calibration PCB

Layer 1 – Plated Through Hole Via Printed Circuit Board
Figure B.54 – Layer 1 Plated Through Hole Via Printed Circuit Board

Layers 2, 4, 5, and 7 – Plated Through Hole Via Printed Circuit Board

Figure B.55 – Layer 1 Plated Through Hole Via Printed Circuit Board
Layer 3 – Plated Through Hole Via Printed Circuit Board

Figure B.56 – Layer 3 Plated Through Hole Via Printed Circuit Board

Layer 6 – Plated Through Hole Via Printed Circuit Board

Figure B.57 – Layer 6 Plated Through Hole Via Printed Circuit Board
Layer 8 – Plated Through Hole Via Printed Circuit Board

Figure B.58 – Layer 8 Plated Through Hole Via Printed Circuit Board
The quasi-static verification in Chapter V used closed form solutions to determine the validity of the simulation output. Ramo, Whinnery, and Van Duzer derived the closed from solutions in ’Fields and Waves in Communication Electronics’. The derivation for capacitance and inductance for a coaxial transmission line with an inner conductor radius $a$ and an outer dielectric radius $b$ are as follows:

**C.1 - Capacitance**

The electric potential for a coaxial transmission line is given by

$$\Phi_r = \ln\left(\frac{r}{b}\right)$$

(E-1)

The radial electric field is

$$E_r = \left(\frac{1}{r}\right) \frac{1}{\ln\left(\frac{a}{b}\right)}$$

(E-2)

From Gauss’s Law, the charge per unit length of the center conductor in the coaxial transmission line is

$$\frac{Q}{\ell} = \frac{2\pi\varepsilon}{\ln\left(\frac{b}{a}\right)}$$

(E-3)
With a delta in potential between conductors chosen to be 1, the capacitance per unit length is found to be

\[ \frac{C}{\ell} = \frac{2\pi e}{\ln \left( \frac{b}{a} \right)} \]  \hspace{1cm} (E-4)

**C.2 - Inductance**

For \( r \) less than \( b \) and greater than \( a \), the magnetic field created by a current \( I \) flowing in the inner conductor and returning on the outer conductor in a coaxial transmission line is given by

\[ H_\phi = \frac{I}{2\pi r} \]  \hspace{1cm} (E-5)

Per unit length, the magnetic flux between \( a \) and \( b \) is

\[ \oint B \cdot dS = \int \mu \left( \frac{I}{2\pi r} \right) dr = \frac{\mu I}{2\pi} \ln \left( \frac{b}{a} \right) \]  \hspace{1cm} (E-6)

Inductance is defined as

\[ L = \frac{1}{I} \oint B \cdot dS \]  \hspace{1cm} (E-7)

Thus, the inductance per unit length is found to be

\[ L = \frac{\mu}{2\pi} \ln \left( \frac{b}{a} \right) \]  \hspace{1cm} (E-8)
LIST OF REFERENCES


