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An experimental and finite element investigation of thermally induced inelastic deformation of single-level damascene copper high density interconnect structures

Nazri B. Kamsah
University of New Hampshire, Durham

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AN EXPERIMENTAL AND FINITE ELEMENT INVESTIGATION OF THERMALLY INDUCED INELASTIC DEFORMATION OF SINGLE-LEVEL DAMASCENE COPPER HIGH DENSITY INTERCONNECT STRUCTURES

BY

NAZRI B KAMSAH

Diploma, Universiti Teknologi Malaysia, Malaysia, 1980
B.Sc. (Hons.), Sunderland Polytechnic, United Kingdom, 1983
M.Eng., Universiti Teknologi Malaysia, Malaysia, 1991

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This dissertation has been examined and approved:

Dissertation Advisor, Todd S Gross
Professor of Mechanical Engineering

Igor I Tsukrov
Assistant Professor of Mechanical Engineering

James E Krzanowski
Associate Professor of Mechanical Engineering

M Robinson Swift
Professor of Mechanical Engineering

Olof E Echt
Professor of Physics

05-04-2001
Date

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ABSTRACT

AN EXPERIMENTAL AND FINITE ELEMENT INVESTIGATION OF THERMALLY INDUCED INELASTIC DEFORMATION OF SINGLE-LEVEL DAMASCENE COPPER HIGH DENSITY INTERCONNECT STRUCTURES

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University of New Hampshire, May 2001

An atomic force microscope was used to investigate thermally induced deformation mechanisms in the areas of copper and polyimide vias in copper-polyimide interconnect structure, as a result of a thermal cycle to 350°C. The copper films exhibited evidence of copper grain boundary sliding, *Coble* creep, and voids formation. Cu-Ta interfacial sliding was observed in the Cu and polyimide via areas. The direction of the Cu-Ta sliding changes as the polyimide via size decreases. The polyimide experienced a residual deformation attributed to the Cu-Ta sliding and in-plane deformation of the copper vias.

A finite element method was used to simulate the effect of Cu-Ta sliding on interfacial and liner plane stresses in *Benzocyclobutane* (BCB)-Cu and SiO_2-Cu interconnect structures, heated to 400°C. A one nm thick element was used to produce a sliding effect at the Cu-Ta interface and at Cu grain boundary. The shear stresses in the SiO_2-Cu system are completely relaxed by the Cu-Ta sliding. The Cu-Ta sliding increases the Ta liner plane stress in the BCB-Cu system to potentially damaging values, while the Ta stress in the SiO_2-Cu system changes from tensile to compressive. Sliding at Cu grain boundary has a minor impact on Cu-Ta sliding and shear stress relaxation in the BCB-Cu system with large aspect ratio.

A finite element technique was used to model the classical *Nabarro-Herring* creep in 1 μm square copper grain subjected to biaxial stresses of ± 10 MPa, at 800°C. A linear elastic mechanical analysis was carried out to simulate the mechanical loading and *transient* thermal analysis was utilized to simulate the diffusive vacancy flow process. The steady state *flux* components were used to predict the creep deformation of the grain and to estimate the creep strain rate at the boundaries. It was shown that the finite element procedure is capable of modeling the *Nabarro-Herring* creep, satisfactorily. The finite element result agrees with the analytical prediction within a factor of two.

Chapter 1

INTRODUCTION

1-1 Integrated Circuit Microchip

Integrated circuit (IC) microchips such as microprocessors, memory modules, and application specific integrated circuit (ASIC) chip are fabricated from vast collections of transistors arranged in different patterns so that they can accomplish different tasks. The transistors that are located in the first level are a complex construction of silicon, metal, and impurities precisely located to create millions of minuscule on-or-off switches that make up the brains of the microchips. **Fig. 1-1** shows a schematic illustration of a complementary metal-oxide semiconductor (CMOS) transistor.

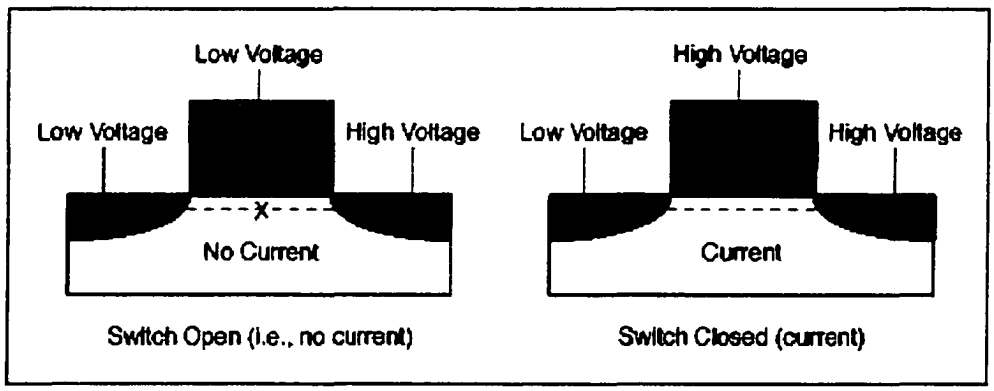


Fig. 1-1 A schematic of a *CMOS* transistor, (a) switch is in an *open* position, blocking flow of electrical current, (b) switch in a *close* position, allowing flow of electrical current across the *silicon*.

Stacked above the base layer of transistors are several layers of conductive metal wiring, which are used to link up the transistors to each other to form circuit elements for the IC microchips. These wiring stacks are known as the high density interconnects (HDIC). The semiconductor industry has used aluminum wiring on IC chips for over 30 years. However, as the size of the CMOS transistors continues to shrink and greater number of transistors are fabricated on a single IC chip to boost up performance and clock speed, the aluminum wiring starts to create problems since its resistance to the flow of electricity increases as the wires are made ever thinner and narrower. The physical limitation on the number of transistors that can reside in a single IC chip is caused by how narrowly manufacturers can focus the beams of light used to etch away transistor components that are made of light-sensitive materials. The largest number of transistors that were integrated in a single chip is, at present, reported to be 32 million [1]. **Fig. 1-2** shows examples of three common IC microchips: a memory module, a microprocessor, and application specific integrated circuit (ASIC) chip.

1-2 Functions of On-Chip Interconnects

The functions served by interconnect metal wirings in IC microchips fall into four categories. The first, called *local* interconnections are used to wire a cluster of adjacent transistors into circuit elements, such as the storage nodes of a static random access memory (SRAM) chip or logic elements in logic chips. The

second type called *global wirings,* are used to connect the circuit elements to form integrated circuits that would carry out specific functions. The most demanding use of such wires occurs in logic arrays where the interconnect wires may span the full extent of the chip. It is these longest metal lines that limit the overall clock speed of the IC microchips.

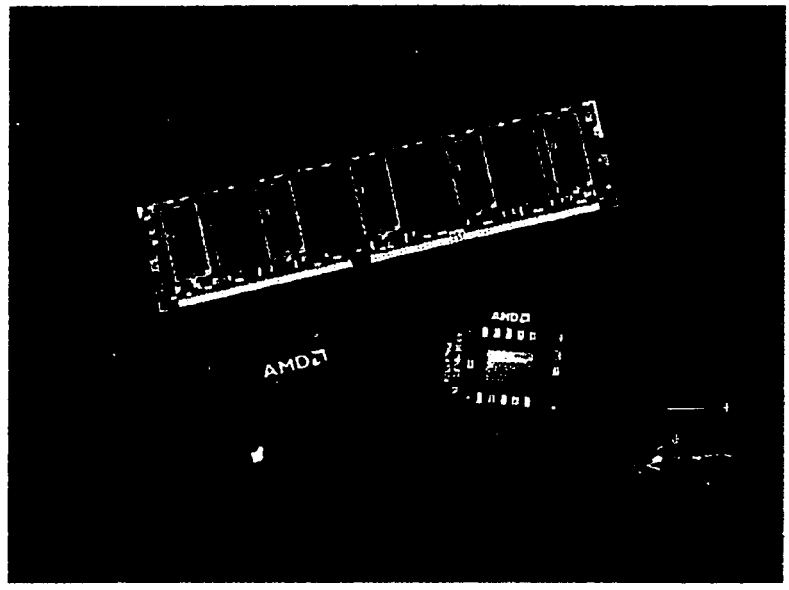


Fig. 1-2 Examples of integrated circuit (IC) microchips (clockwise from top): a random access memory (RAM) module, a microprocessor, and an application specific integrated circuit (ASIC) chip.

The third type is the metal interconnects that carry power to the transistors and circuit elements on the chip. Lastly, there is the interconnection level, which acts as an interface with a packaging element on which a number of IC chips are mounted and interconnected, which may be in the form of bonding pads or array of solder bumps. **Fig. 1-3** shows an example of older wiring architecture used in a static random access memory (SRAM) array. The first

interconnection level or base structure is shown in pink color while the colored yellow metal is the first level of global interconnection. The insulating dielectric has been removed, thus revealing the underlying interconnection structures.

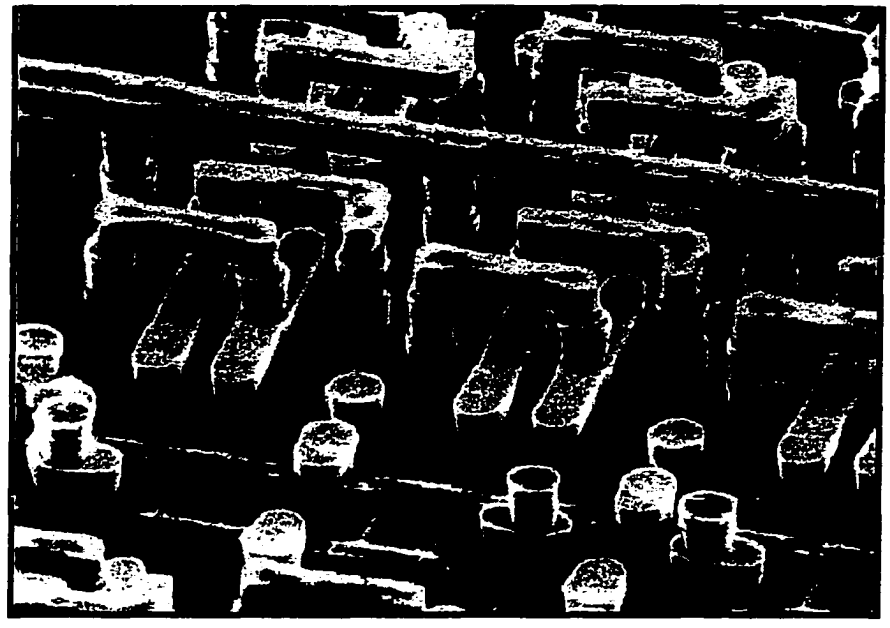


Fig. 1-3 A scanning electron micrograph of a portion of a static random access memory (SRAM) array. The *local* interconnections (*tungsten;* colored pink) provide cross coupling for the *n*+ and *p*+ diffusion contacts and act as the lower portion of the contact studs to the first *global* interconnection level (*Ti/Al(Cu)/Ti/TiN;* colored yellow). The contact studs (*tungsten;* colored light green) constitute the upper portion of the contact paths to the global interconnections. (*Copyright 1995 IBM Corporation*).

Fig. 1-4 shows an example of a new back end-of-the line (BEOL) wiring architecture used in a complementary metal-oxide semiconductor (CMOS) logic chip, developed by IBM. The arrow indicates the local interconnection layer at the bottom. Three levels of global interconnection structures are shown above the local interconnection layer.

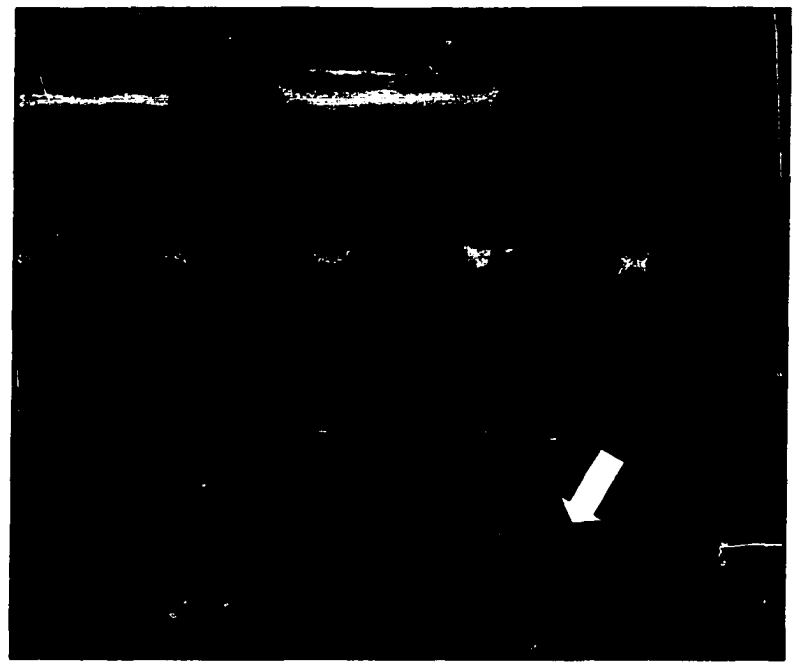


Fig. 1-4 A scanning electron micrograph of cross-section of a portion of a 0.5 μm CMOS logic chip developed by IBM. The arrow shows the local interconnection structures at the bottom level. Three levels of global interconnections are also shown. (*Copyright 1995 IBM Corporation*).

1-3 Scaling of On-chip Interconnects

The numbers of transistors contained in a single chip have quadrupled every 3-4 years [2]. The size of IC chips has been increased by a factor as large as 1.3, and to make this trend possible the minimum linear feature size has been reduced by a factor of approximately 0.7. The metal interconnect wires on IC chips in current production are expected to shrink in size by a factor of 2 every six years over the next 15 years, from about 700 nm in 1997 to 140 nm by the year 2012. Shrinking the sizes of components has allowed greater numbers of chips to be fabricated on each wafer, increasing efficiency and reducing cost. However, as

the IC structures are scaled to smaller dimensions, fabrication process becomes more complex. Increasing the number of transistors that reside in a single IC chip leads to the need for greater number of interconnect wiring levels, especially in the logic IC chips. It was reported that at present, integrated circuits are composed of five layers in which each layer is about 1 μm thick [3]. By the year 2012 IC chips with eight layers of on-chip interconnect wirings should be common and metal structures within integrated circuits will have an aspect ratio (width to height) as large as 10:1.

Increasing the number of wiring levels causes signal propagation delay due to on-chip wiring to become more dominant than that due to the active silicon devices. The use of more interconnect wiring levels also leads to an increase in the number of processing operations. As the device dimensions approach sub half-micron size, the scaling of geometries causes an increase in interconnection resistance and current density. The increase in current densities in the finer dimensions devices lead to increased concern for reliability.

1-4 New Materials for IC Interconnects

Improvement of the performance of on-chip IC interconnection requires a substitution of new materials with lower resistivity. Metal wirings used in traditional IC interconnect wires are aluminum (Al), which is doped with about 1 % copper (Cu) to improve its resistance to *electromigration* (the atomic diffusion

flux caused by the momentum exchange between electrical charge carriers and diffusing atoms, which occurs primarily along the grain boundaries in polycrystalline-type interconnects). Tungsten vias are used as interlayer contacts. The Al is placed in a titanium liner, which acts as a shunt and a barrier layer, and the whole structures are embedded in silica.

Although aluminum has long been the material for the interconnect metal wires in the IC chips, it will soon reach the technological and physical limits of the existing semiconductor technology due to the continuous shrinking of the IC chips. At and beyond the 0.25 μm device dimensions, the chip's performance is limited by the interconnect signal propagation delays, signal dispersion, and/or crosstalk noise associated with the Al-SiO_2 material system that is used at present. The interconnect propagation delays and capacitive crosstalk noise can be reduced by replacing aluminum with copper and the SiO_2 insulator with a low-*k* dielectric material. For a given speed performance, the combination of copper and low-*k* dielectrics enable a reduction of the number of interconnect levels compared to the aluminum and silicon dioxide interconnect material system, resulting in reduced manufacturing cost and improved chip reliability [4]. For a specified number of interconnect levels, the combination of copper and low-*k* dielectrics provides higher chip speed performance compared to the Al-SiO_2 interconnection system.

Recent introduction of IC chips using copper-based metallization, lead by IBM, has marked the beginning of a change from aluminum to copper metallization technology in the semiconductor industries. Copper has many advantages over the traditional Al-alloy interconnect wires used at present. Its lower resistivity ($\approx$ 1.67 $\mu\Omega$cm vs. 2.65 $\mu\Omega$cm for Al(Cu) alloy) allows finer wires with lower resistive losses, resulting in shorter on-chip resistance-capacitance (RC) time delays [5]. In addition, copper has higher mass density and melting point temperature, making it significantly less susceptible to electromigration than aluminum. Also, it is less likely to fail under stress. The use of copper wiring thus enables higher IC chips speed, enhance electromigration lifetime reliability, reduce power consumption, and ultimately reduce manufacturing cost for IC chips. Another advantage is, it is relatively easier to obtain a clear interface in copper than in aluminum, a factor that can be important in fabrication of multilevel interconnection systems, since this can greatly reduce contact resistance between the various wiring levels.

To be used successfully as a new metal conductor in the IC microchips, many problems associated with copper integration need to be solved first. One major problem with Cu integration has been the difficulty in carrying out dry etching processes on the Cu films at room temperature. Copper also has a poor adhesion characteristic to the dielectric material and it oxidizes easily to form copper oxide, which increases its resistivity. Copper atoms can easily diffuse into the silicon substrate, which can cause deep level defects by the formation of

copper silicide, at temperatures as low as 200 °C [6]. This phenomenon would alter the desired semiconducting properties of the silicon, resulting in the degradation of the IC devices. Thus, to make copper interconnect wires feasible for integration in IC microchips, an effective diffusion barrier is imperative. Tantalum (Ta) and tantalum nitride have been demonstrated to be successful in preventing the diffusion of the Cu atoms into both the Si substrate and the SiO_2 dielectric, and simultaneously improve the adhesion of the Cu to both materials. Tantalum is a highly refractory metal with a melting point temperature of about 3000 °C [7]. Another important benefit of using the Ta as the diffusion barrier is that, it does not forms Cu-Ta compounds when integrated with copper.

1-5 Fabrication Process of Copper Interconnect

Process integration of copper and low-*k* dielectrics requires relatively conformal processes for the copper and diffusion barrier, chemical-mechanical polishing (CMP) to form the inlaid copper lines-plugs and suitable low-*k* dielectrics. The present trend in IC fabrication is towards using the damascene process, but mainstream copper metallization fabrication is based on a dual-damascene process. Fabrication of each damascene interconnect level involves formation of the metallization via holes and metal trenches by a sequence of microlithography patterning and anisotropic dielectric reactive ion etching (RIE) process steps, performed sequentially twice. Using the dual-damascene process, the inlaid copper via plugs and metal lines are then formed through deposition

of a continuous diffusion barrier layer, followed by void free filling of the via holes and metal trenches using a suitable copper deposition method. The following sections present a brief description of these processes.

1-5-1 Damascene Metallization Technique

Fig. 1-6 illustrates the steps involved in the damascene metallization process for fabricating a single level copper interconnect structure.

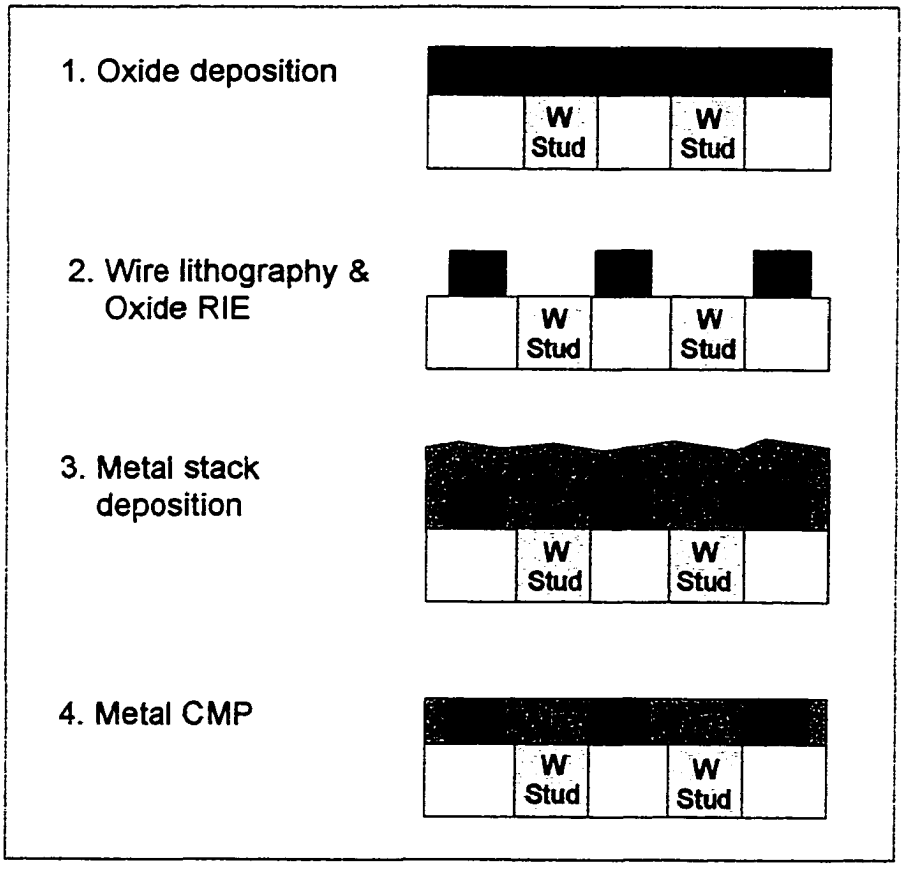


Fig. 1-5 A simplified schematic showing the steps involved in the damascene metallization process, for fabricating a single level copper interconnect structure.

The first step is to deposit a low-*k* dielectric layer on a planar silicon (Si) substrate surface. Then, wire recess pattern is formed in the dielectric by microlithography, in which the structure is first coated with a photoresist material. Next, the pattern is exposed to a ultra-violet (UV) light source. The unexposed photoresist material is then removed by using chemical developer while the exposed dielectric is etched out by reactive ion etching (RIE). Following the dielectric patterning, a 30-200 nm thick tantalum (Ta) liner is then deposited on the structure at an elevated temperature (not schematically shown in *Fig. 1-5*), to improve Cu adhesion to the dielectric and to prevent the diffusion Cu atoms into the Si substrate and the dielectric.

After the pattern definition process is completed, copper is deposited to fill up the metal trenches. Examples of the copper deposition techniques will be briefly described in *Section 1-5-3*. In the final step, the excess metal on the surface of the structure is removed using a planarization method such as chemical-mechanical polishing (CMP). This step results in a planarized wiring and via, embedded in the dielectric. In the fabrication of a multilevel interconnection system, the above steps are repeated on top of the first interconnection level structure. The *damascene* process is ideally suited for fabricating copper interconnection systems since it allows the inlaying of the metal simultaneously in the vias and the overlying line trenches.

1-5-2 Dual-damascene Metallization Technique

In a dual-damascene metallization, a monolithic stud-wire structure is produced from the repeated patterning of a single thick dielectric film, followed by metal filling and planarization. A simplified schematic in **Fig. 1-6** shows the steps involved in the dual-damascene metallization. First, a relatively thick dielectric layer is deposited on a planar Si substrate surface. The thickness of the dielectric is slightly larger than the final desired thicknesses of the stud and wires, since a small amount will be removed during the polishing step using CMP. Stud recesses are formed in the dielectric using photolithography and reactive ion etching (RIE) that either partially drills through the dielectric or traverses the dielectric and stops on the underlying metal to be contacted. Wire recesses are then formed using a separate photolithography and a timed dielectric-etching step. If the former stud RIE option is used, the wire etching completes the drilling of the stud holes. Alternatively, the wire recess can be formed first, but this approach makes photolithography for the stud to become more difficult, since the resulting surface is less planar.

In the following step, the stud-wire metallization is deposited and then planarized by chemical-mechanical polishing (CMP). The resulting interconnect structures are less expensive to fabricate since one dielectric deposition step, one metal deposition and one dielectric planarization CMP step have been avoided.

In addition, contact resistance between the wire and the underlying stud is eliminated since there is no interface within the monolithic structure.

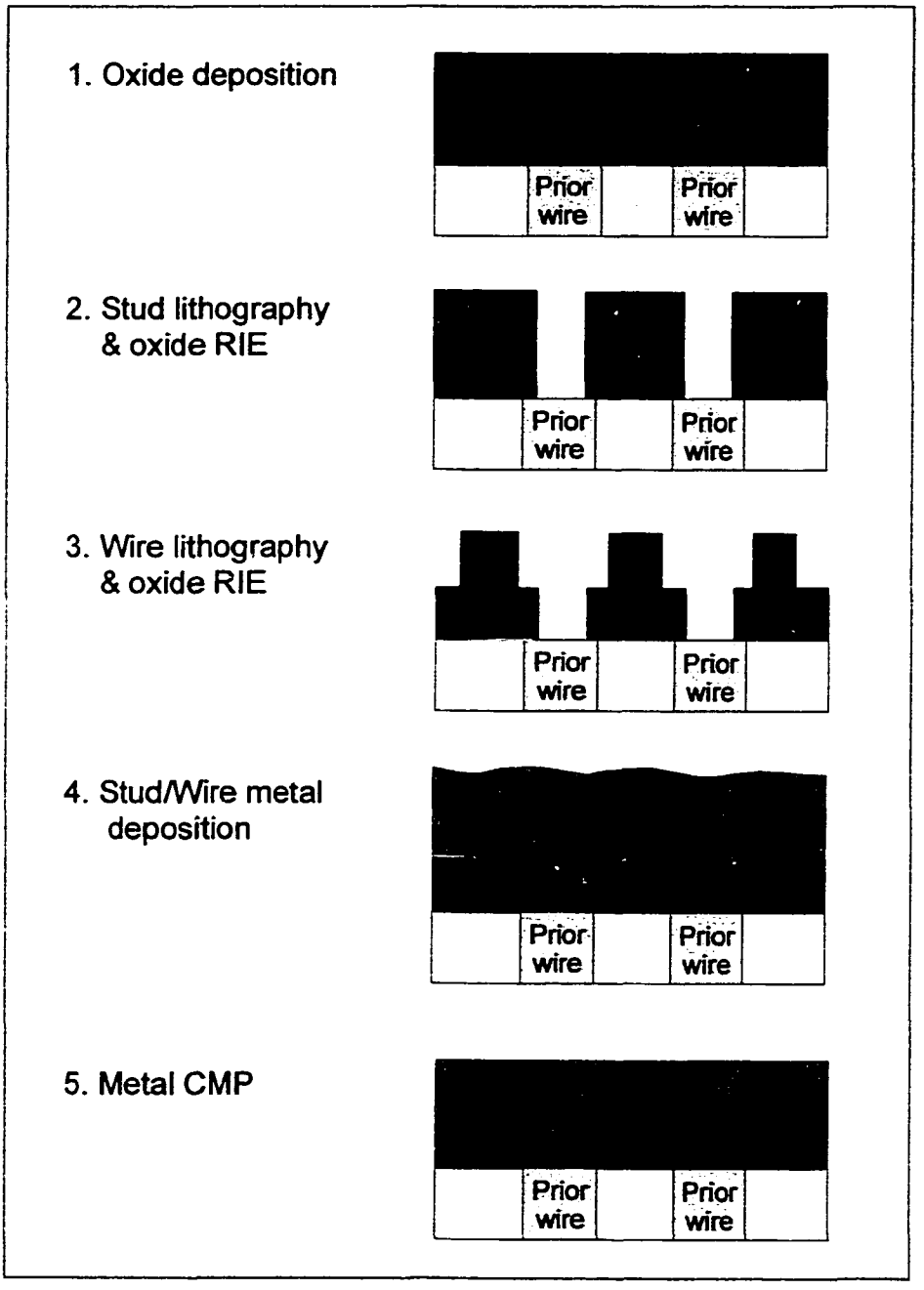


Fig. 1-6 A simplified schematic illustrating the process steps involved in the fabrication of a dual-damascene copper interconnect wiring.

1-5-3 Copper Deposition Techniques

Copper deposition in damascene and dual-damascene metallization could be accomplished by various methods such as collimated sputtering, ion cluster beam, electron cyclotron resonance (ECR), physical vapor deposition (PVD) and plasma-enhanced chemical vapor deposition (PECVD). The collimated sputtering method is particularly suitable for depositing thin film liner to cover features having moderate aspect ratios. A much simpler method such as electrochemical plating could also be used to deposit copper into the defined wire trenches. Electrochemical plating has several advantages compared to PVD and CVD due to its low cost, low processing temperature, and its excellent ability to fill-up via trenches. Electroplating therefore has become the leading technique for copper metallization in future ultra large-scale integration (ULSI) interconnection systems [8]. Before the copper can be deposited into the trenches, it is necessary to cover the surface with a blanket film of seed layer material. Such layer is needed because of the difficulty in nucleating copper on the liner, which is exposed to ambient air. The primary function of this layer is to conduct electrical current from a contact at the wafer edge to all points on the wafer, where copper deposition is desired.

The requirement of a seed layer in copper metallization by electroplating has led to a variety of approaches. Two most popular approaches are through-mask and damascene plating. The through-mask plating utilizes a masking

material covering the seed layer. Electroplating occurs only on those areas of the seed layer that are not covered by the mask. The masking material and the surrounding seed layer are subsequently removed. As opposed to the through-mask plating, the seed layer in damascene plating is deposited over a patterned dielectric material. The plated metal covers the entire surface of the dielectric. After depositing the seed layer, the metal is deposited using the same electroplating technique.

Continuous copper seed layers are essential for electroplating deposition to completely fill the trench and/or via patterns. This requirement places extreme demands on the ability of the seed layer to conform to the geometries of the structures to be filled. The damascene structures typically have trenches of 0.4 μm wide or less and vias of similar diameter [9]. Such geometry, when combined with dielectric layers greater than 1 μm thick, can drive the aspect ratio of the structure to 3:1 or greater.

1-6 Objective and Scope

1-6-1 Inelastic Deformation of Copper-Polyimide Interconnect Structure

During the fabrication of copper interconnect structure the various material components of the structure are subjected to a heating to elevated temperatures as high as 400 °C. In the manufacturing of a multilevel copper interconnection system, the structure of the first interconnection level may be

subjected to several heating and cooling cycles to elevated temperatures. Thermal stresses are developed in the structure during the heating cycles, owing to a mismatch in the coefficient of thermal expansion (CTE) between the silicon substrate, dielectric, diffusion barrier liner and copper conductor. At high temperatures, the metal components of the structure undergo inelastic deformation to relief the stresses. Such deformation may cause failure at the interfaces between the various interconnection levels, at the interface of the metal contact studs, and decohesion failure at the vertical interfaces. These would have a severe impact on mechanical integrity of the structures during the fabrication process and thus becomes a reliability issue.

Thermally induced deformation of parallel line arrays in a single level copper-polyimide interconnect structure as a result of a 25°C-350°C-25°C thermal cycle has been reported by *Zhmurkin* [10]. The copper film was shown to exhibit heterogeneous deformation, showing evidence of Cu grain boundary siding resulting in large Cu grain build up and a relative step height at Cu grain boundary, and *Coble* creep mechanism leading to what look like decoration at the Cu grain boundary. In addition to these "classical" high temperature deformation mechanisms, interfacial sliding at the copper-tantalum interface was also observed. The heterogeneous deformation of the copper film could lead to a mechanical failure of the structure due to delamination of the interlayer dielectric and decohesion of the dielectric at vertical interfaces.

Chapter 2 reports an experimental work on thermally-induced inelastic deformation in a 1 μm thick single level copper-polyimide interconnect structure as a result of a similar 25°C-350°C-25°C thermal cycle. The goal is to investigate the mechanisms of the deformation of the areas of copper and polyimide via structure. In a multilevel Cu-polyimide interconnect structure, the vias are used as contact studs for connecting the various wiring levels. The surface topography around the area of copper and polyimide vias was recorded before the thermal cycle using a Dimension 3000 atomic force microscope (AFM) operating in TappingMode™. Images were acquired at several different scan sizes to study local and larger scale deformation behavior of both Cu vias in a polyimide film and polyimide vias in copper background.

The test specimen was heated from 25°C to 350°C at a rate of 2°C/minute and then cooled back to 25°C at the same rate, in a nitrogen environment to prevent oxidation of copper. Immediately after cooling, the surface topography of the same via areas was carefully acquired using the TappingMode™ AFM, taking care to match the lateral orientation. Then, the image of surface topography obtained before the cycle was subtracted from the image of the same area acquired after the thermal cycle, so that the resultant topographical image represents the *out-of-plane* deformation map of the via structure due to the thermal cycle. The deformation maps are then utilized to show evidence of high temperature deformation mechanisms in the structure.

1-6-2 Effects of Cu-Ta Sliding on Interfacial and Liner Plane Stresses

As mentioned earlier, during the fabrication of a multilevel copper interconnection system the existing wiring layers may be subjected to several thermal cycles to 350 °C. Thermal stresses are developed in the structure due to mismatch in the coefficient of thermal expansion (CTE) between various material components of the structure. The stresses are often quite large and may exceed the yield strength of the metallic material components [11], and they could cause structural failure due to metal cracking, stress-induced voiding and interfacial failure by delamination at the vertical interfaces of dissimilar materials. As the existing interconnection layers are heated to the peak processing temperature (around 350°C to 400°C), copper is subjected to a significantly high homologous temperature (about 0.45 T/T_m, where T_m is the melting temperature for copper). This enables a *diffusion-accommodated* interfacial sliding to operate at the copper-tantalum interface, to relief the interfacial shear stresses [12].

The phenomenon of interfacial siding at the Cu-Ta interface of parallel Cu line arrays in a copper-polyimide interconnect structure as a result of 25°C-350°C-25°C thermal cycle was reported by *Zhmurkin* [10]. It was demonstrated that the Cu-Ta sliding results in relaxation of the out-of-plane shear stresses at the interface. Evidence of Cu-Ta interfacial sliding was also observed in the experimental investigation of inelastic deformation in Cu-polyimide interconnect structure, as reported in *Chapter* 2.

A finite element (FE) modeling of the Cu-Ta interfacial sliding in parallel Cu line arrays in a 1 μm thick single level copper-polyimide interconnect structure was also reported by *Zhmurkin* [10]. The Cu-Ta sliding effect was produced by using a 1 nm thick sliding element, incorporated into the finite element models between copper and the tantalum liner. The sliding rate of the element was calibrated so that it matches the steady-state creep strain rate predicted using an analytical model proposed by *Raj and Ashby* [13]. During the FE simulation, the structure was heated to elevated temperatures ranging from 50°C to 350°C, to investigate the effect of the Cu-Ta sliding on the stress-time behavior. It was shown that at all temperatures, the sliding caused the out-of-plane shear stress at the interface to relax. Although the FE simulations were not performed for the full period necessary to completely relax the shear stresses, it was demonstrated that the stress-temperature data fits well to an exponential function.

In this study, the FE simulation of Cu-Ta sliding similar to that reported by *Zhmurkin* [10] is being extended to copper interconnect structures having different dielectric materials. *Chapter 3* describes the use of a plane strain finite element technique to simulate the Cu-Ta interfacial sliding in a 1 μm thick single level *Benzocyclobutane* (BCB)-copper and SiO_2-copper interconnect structures as a result of heating from 20 °C to 400 °C, assuming that the structures are stress free at 20 °C. Finite element models of the BCB-Cu and SiO_2-Cu structures were

constructed using isoparametric 4-node quadrilateral elements and a 1 nm thick sliding element was incorporated into the finite element models (between copper and tantalum) to produced the Cu-Ta sliding effects. The sliding model used previously by *Zhmurkin* [10] was adopted. The goals of this study are to estimate the thermal stresses developed in the structures at 400°C and to predict the effect of the Cu-Ta sliding on the interfacial and liner plane stresses. The effects of the sliding on the stresses were evaluated by comparing the *relaxed* and *unrelaxed* stress states. The effects of line width-to-thickness (*w/t*) aspect ratio and Ta liner thickness on the thermal stresses were also investigated.

It was also reported by *Zhmurkin* [10] that while Cu-Ta sliding was observed in 1 μm wide lines, little or no sliding was observed in 10 μm wide lines. It was proposed that, sliding at Cu grain boundary suppresses the Cu-Ta sliding in the wider lines and provides an alternative path for the relaxation of interfacial shear stresses. In this study, FE simulation is utilized to simulate the effect of Cu grain boundary sliding in a BCB-Cu structure having large aspect ratio and thin Ta liner. The goal is to evaluate the effect of the sliding on the Cu-Ta interfacial sliding and the relaxation of out-of-plane shear stress at the BCB-Ta interface. The sliding effect was produced using the same 1 nm thick sliding element as for generating the Cu-Ta sliding, except that the sliding rate is twice as fast, because both sides of the interface contribute to the sliding.

1-6-3 Finite Element Modeling of Classical Nabarro-Herring Creep

Chapter 4 describes the use of finite element (FE) procedure to model the classical *Nabarro-Herring* creep in a 1 μm square copper grain subjected to biaxial stresses of ± 10 MPa at 800 °C. The goal of this study is to establish a rigorous numerical method to describe localized deformation of copper, based on adaptation of the *Nabarro-Herring* creep model. The FE procedure can be used to make more realistic estimates of the thermomechanical stresses developed in the copper interconnection structures. Finite element models of the Cu grain were constructed using isoparametric 4-node quadrilateral element, which was then discretized into 50 x 50 divisions. A linear elastic mechanical analysis was carried out using MARC-Mentat finite element software to simulate the mechanical loading and to produce the elastic deformation of the grain. The diffusive vacancy flow process was simulated using *transient* heat transfer analysis function of the FE software because the equations for diffusional vacancy flow process are identical to those for heat conduction.

A finite element (FE) procedure for modeling the *Nabarro-Herring* creep phenomena in copper grain was proposed earlier by *Wu* [14]. In this procedure, the new steady-state vacancy concentration at the boundaries was utilized to produce the volumetric dilatation of the grain to represent the deformation of the grain due to vacancy flow creep, and to estimate the steady-state creep strain rate. In this study, the previously proposed FE procedure was re-evaluated and

earlier simulation result was shown to be three orders of magnitude lower than the prediction of the classical *Nabarro-Herring* model. Modifications were made to the FE procedure to improve its overall performance. In the modified FE procedure, the nodal displacements computed based on the components of vacancy flux at all nodes, were utilized to predict the creep deformation of the grain and to estimate the steady state creep strain rate at the boundaries of the grain. The validity of the modified procedure was verified by evaluating the deformed shape of the grain due to creep and by comparing the steady state creep strain rate with that predicted by the classical *Nabarro-Herring* model.

Chapter 2

EXPERIMENTAL METHOD

An atomic force microscope (AFM) was employed in an experimental investigation of thermally-induced inelastic deformation of a copper-polyimide interconnect structure as a result of a thermal cycle to 350 °C. The details of this study will be presented in *Chapter 3*. One important advantage of AFM over other existing microscopes is that the image is acquired as a digital three-dimensional data. One can therefore conducts a thorough analysis such as surface roughness, height and depth measurements, grain size analysis, etc. This chapter presents a brief overview of the AFM, which is a family member of the scanning probe microscopes (SPMs).

2-1 Overview of Scanning Probe Microscopy

Scanning probe microscopes (SPMs) are a family of instruments used to measure properties of surfaces. In their first applications, SPMs were used solely for measuring surface topography and, although they can now be used to measure many other surface properties, measurement of surface topography is still their primary application. The main feature that all SPMs have in common is that the measurements are performed with a sharp probe scanning over the surface while maintaining a very close spacing to the surface. This produces an

atomically short depth of focus such that only the top layer of rigidly bound atoms is seen. Excellent spatial resolution can be obtained by using a very sharp probe (on the order of a few nanometers radius of curvature and with a very steep sidewall angle) and keeping it's spacing from the surface very small (usually within a nanometer). SPMs are most commonly used to perform very precise, three-dimensional measurements on the nanometer to micron scale. The lateral resolution of the SPMs is typically 20 Å. More advanced instruments can have lateral resolution better than 1 Å. The Z resolution of most SPMs is typically in the order of 1 Å [15].

2-2 Basic SPM Components

2-2-1 Scanning System

The scanner is the most fundamental component and the heart of the scanning probe microscopes. Depending on its design, the scanner may scan the sample surface in a raster pattern or the sample is moved under a stationery scanner. A piezoelectric tube scanner is typically used to obtain high precision scanning. It can be controlled to provide sub-angstrom motion increments.

2-2-2 Probe or Tip

Another key component in the system is the probe or tip. The tip is secured at the end of a cantilever. Most cantilevers are manufactured to have spring constants of less than 1 N/m, allowing topographic imaging of material's

surface by sliding the tip-cantilever assembly across the surface and monitoring the deflection of the cantilever. The cantilevers can have resonant frequencies greater than 10 kHz to allow rapid scanning over surfaces with high spatial frequency roughness.

2-2-3 Probe Motion Sensor

A probe motion sensor is used to provide a feedback correction signal to the piezoelectric scanner in order to keep the spacing between the top and the surface of the material being scanned constant. The most common design is a beam deflection system, which uses a laser light shining onto and reflecting off the back of the cantilever and onto a segmented photodiode to measure the probe motion. Other types of feedback systems include interferometers, piezoelectric cantilevers and probe oscillation systems that detect forces by the change in the resonant frequency, phase, or amplitude of oscillation. However, the beam deflection system is the most widely used probe motion sensor because it produces lowest noise and more stable operation.

2-2-4 Electronics and Computer System

The electronic interface unit provides an interfacing between the scanning system and the computer system. The unit supplies voltage that controls the piezoelectric scanner, accepts the signal from the probe motion sensor unit and contains the feedback control system for maintaining the constant spacing between sample and tip during the scanning. Scanning probe microscopy would

not be feasible without the availability of a computer system to drive the scanning system, to process, display, store, manipulate and analyze the acquired topographical data.

2-3 Atomic Force Microscope

The development of an atomic force microscope (AFM) was preceded by the introduction of the Scanning Tunneling Microscope (STM) in 1981, at IBM Research Laboratory in Zurich, Germany [16]. Although the STM provides subangstrom resolution in all three dimensions, its usage is limited to conductive and semiconductive samples.

Fig. 2-1 The essential components of Digital Instrument *Dimension 3000* atomic force microscope. (Adapted from [18]).

The atomic force microscope (AFM) was first developed in 1986 [17] for imaging insulators as well as conductors. Digital Instruments produced the first commercial AFMs in 1989. The AFMs provide a three-dimensional surface topography of insulators and conductors with lateral resolution on the order of nanometers and subangstrom vertical resolution. The essential components of the Digital Instruments *Dimension 3000* atomic force microscope (AFM) are illustrated in **Fig. 2-1** [18].

2-3-1 Imaging Mechanisms of Atomic Force Microscope

AFM essentially consists of a very sharp tip attached at a free end of a flexible cantilever, as shown in **Fig. 2-2**. The tip is moved in a raster pattern across a sample surface while maintaining a small, constant force.

Fig. 2-2 An example of tip-cantilever assembly typically used as an imaging mechanism in atomic force microscopes (AFMs).

The tips typically have an end radius of 2 nm to 20 nm, depending on the tip type, and the cantilever is typically 100 to 200 μm long. [18]. The scanning motion is conducted by a piezoelectric tube scanner, shown in **Fig. 2-3**, which scans the tip in a raster pattern with respect to the sample (or scans the sample with respect to the tip).

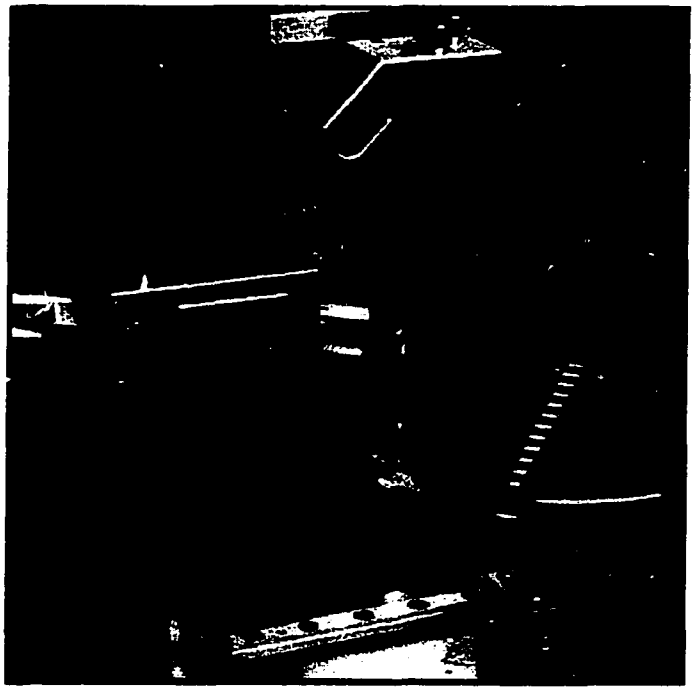


Fig. 2-3 A piezoelectric tube scanner of an atomic force microscope. (Adapted from [21]).

The tip-sample interaction is monitored by reflecting a laser light off the back of the cantilever, into a split position sensitive photodiode detector (PSPD). By detecting the difference in the photodetector output voltages, changes in the cantilever deflection or oscillation amplitude are determined. **Fig. 2-4** shows a schematic of this scheme.

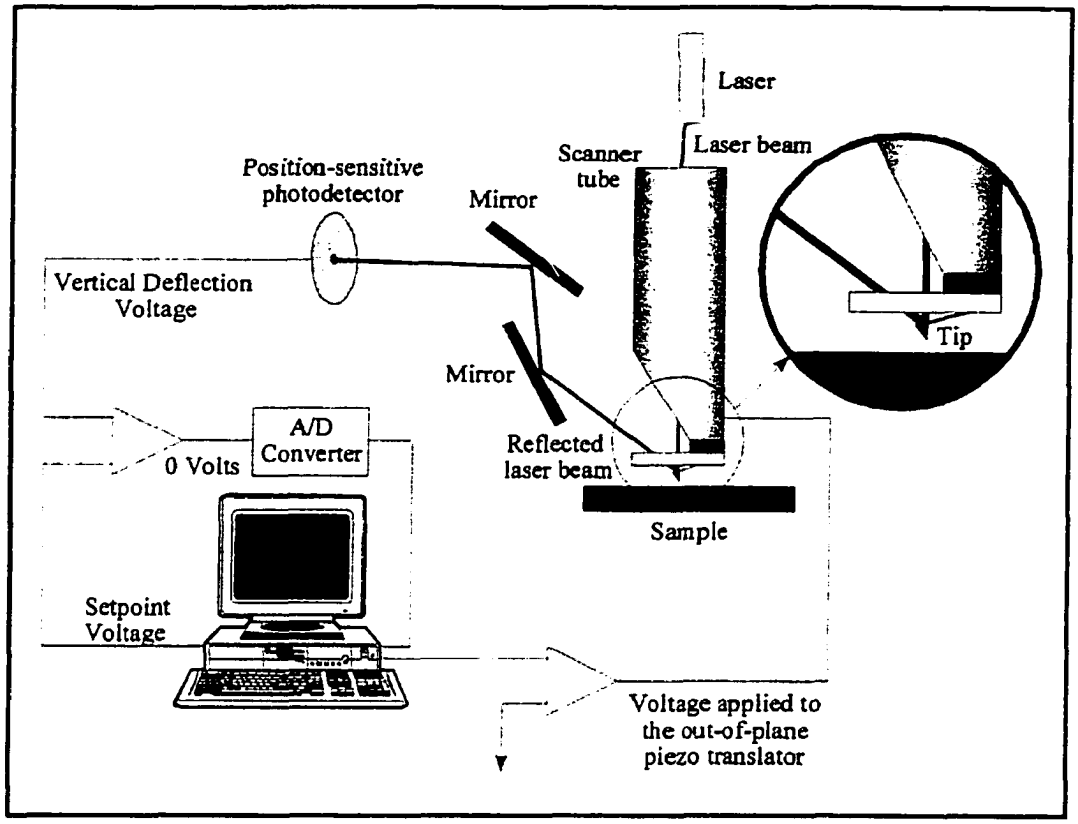


Fig. 2-4 A laser light probe motion sensor is widely used in atomic force microscopy applications.

In a normal operation, the tip scans a flat portion of the sample surface, maintaining the laser beam at the center of the PSPD. As the tip encounters a raised feature, the cantilever and the laser beam are deflected upward into the upper half portion of the PSPD. This portion thus receives an increasing amount of laser light and its voltage increases. The voltage difference is sensed by the feedback electronics, causing a dropped voltage to the Z piezo crystal, and the piezo retracts. As this occurs, the tip is raised until the laser beam is shifted back to the center of the PSPD.

When the tip encounters a decline in the sample topology, the tip drops down. This directs more of the laser beam onto the lower half portion of the PSPD and causes the voltage of that portion to increase. The voltage differential is sensed by the feedback electronics and the voltage to the Z piezo crystal is increased, causing the piezo to extend. As this happens, the tip is lowered until the laser beam is brought back to the center of the PSPD. The voltage differentials are recorded by the computer system and later converted into topographical images of the features measured on the sample surface.

2-3-2 Operation Mode of Atomic Force Microscope

Two most commonly used modes of AFM operation are the contact mode and TappingMode™. Contact mode AFM consists of scanning the probe across a sample surface while monitoring the change in cantilever deflection with the split photodiode motion detector. A feedback loop maintains a constant cantilever deflection by vertically moving the scanner tube to maintain a constant photodetector difference signal. The distance the scanner moves at each x and y data point is stored by the computer system to form the topographic image of the sample surface. The feedback loop maintains a constant force of approximately 0.1 to 100 nN during the scanning.

Contact mode AFM suffers from many drawbacks that limit its applications. The constant downward force of the tip onto the sample surface is not always low enough to avoid damaging some sample surfaces such as

biological, polymer and silicon wafer surfaces. Under typical atmospheric ambient environment, surfaces are always covered by 10 to 30 monolayers of adsorbed gas, consisting of mostly water vapor, hydrocarbons, nitrogen, and carbon dioxide, held on the surface by an interatomic *van der Waals* force. A surface tension associated with the absorbed gas causes the layer to wick up onto the AFM tip when the tip comes into contact with it, as illustrated in **Fig. 2-5**. This pulls the tip toward the surface with a damaging force. As the contact AFM tip rubs across the sample, the tip can also cause sufficient frictional force to produce shear forces that can push and tear surface features.

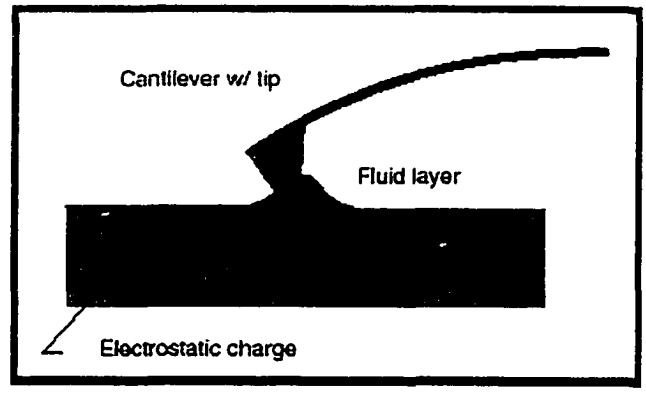


Fig. 2-5 In contact mode AFM, electrostatic and/or surface tension forces from the absorbed gas layer pull the scanning tip toward the sample surface.

TappingMode™ AFM consists of oscillating the cantilever near its resonance frequency (about 300 kHz) and lightly "tapping" on the surface during the scanning. The laser deflection method (see **Fig. 2-4**) is used to detect the root-mean-square (RMS) amplitude of cantilever deflection. A feedback loop

maintains a constant oscillation amplitude by moving the piezoelectric scanner vertically at each x and y data point. The computer system records this movement to form the topographical image of the sample surface. The advantage of TappingMode™ with respect to the contact mode AFM is that it eliminates the lateral shear forces present in contact mode. This enables the TappingMode™ AFM to be used to image soft, fragile, and adhesive surfaces without damaging them, which is difficult to perform using the contact mode AFM.

2-3-3 AFM Scanning Resolution

The lateral resolution of an AFM image is determined by two factors: the image step size and the minimum radius of the probe tip. An image with a scan size of 1μm x 1μm taken with 512 data points per scan line would have a lateral resolution of about 20Å (i.e. 1 μm divided by 512). The sharpest tips available commercially can have a radius as small as 50Å. Because the interaction area between the tip and the sample is only a fraction of the tip radius, these tips typically provide a lateral resolution of 10 to 20Å. The lateral resolution of AFM images larger than 1μm x 1μm is therefore determined by the mage step size instead of the tip radius. Scanning speed is an important parameter in controlling the z-resolution of the AFM images. The feedback control loop, which measures the deflection of the cantilever, has to have enough time to adjust the response of the out-of-plane piezoelectric translator. Therefore, a more superior z-resolution can be achieved with slower scanning speed.

Chapter 3

INVESTIGATION OF THERMALLY INDUCED DEFORMATION OF DAMASCENE COPPER INTERCONNECT STRUCTURE

3-1 Deformation of Copper Interconnect Structure

Experimental investigation of thermally induced deformation of a 1 μm thick single level damascene copper-polyimide interconnect structure as a result of 25°C-350°C-25°C thermal cycle using atomic force microscope (AFM) was reported by *Zhmurkin* [10]. **Fig. 3-1** shows an out-of-plane deformation map of Cu film, showing evidence of high temperature deformation mechanisms resulting from the thermal cycle.

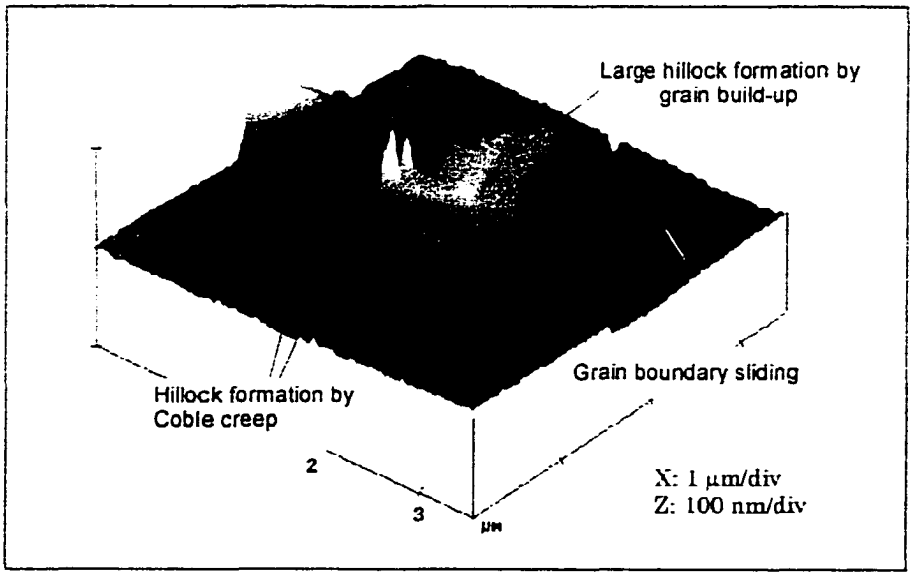


Fig. 3-1 An out-of-plane deformation map of a copper film showing *heterogeneous* deformation as a result of 25°C-350°C-25°C thermal cycle. (Adapted from [10]).

A large hillock due to Cu grain build-up, attributed to flow of matter across the Cu grain boundary from the adjacent grains can be seen at the middle of the image. Decoration at the Cu grain boundary attributed to *Coble* creep is seen at the left side of the image. The step between the Cu grains shown at the right of the image is a result of sliding at Cu grain boundary. In addition to these classical high temperature deformation mechanisms, sliding at copper-tantalum interface was also noted. It results in the polyimide appearing to be held up at the interface. It was proposed that the sliding occurred during the heating cycle and did not completely recover during cooling cycle. A simplified schematic shown in **Fig. 3-2** summarizes the various high-temperature deformation mechanisms that were observed in the structure [10].

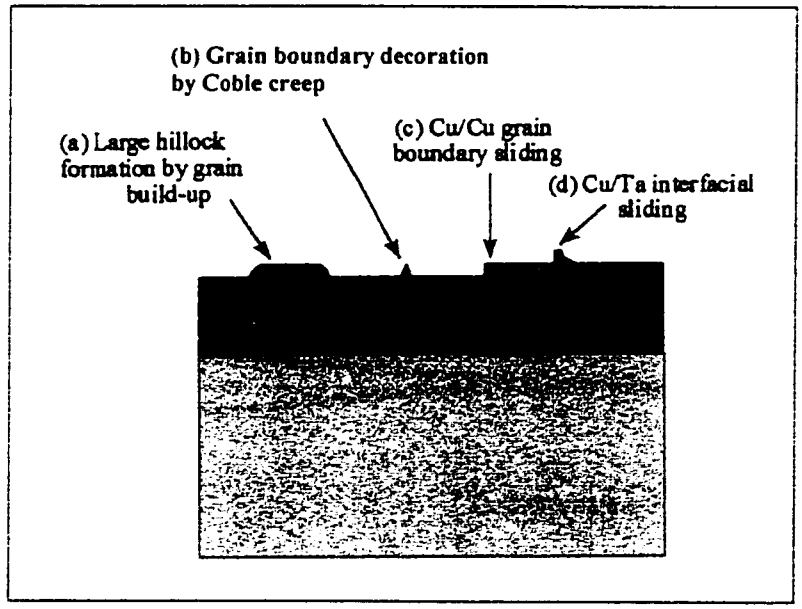


Fig. 3-2 A summary of classical high temperature deformation mechanisms observed in a copper-polyimide interconnect structure. (Adapted from [10]).

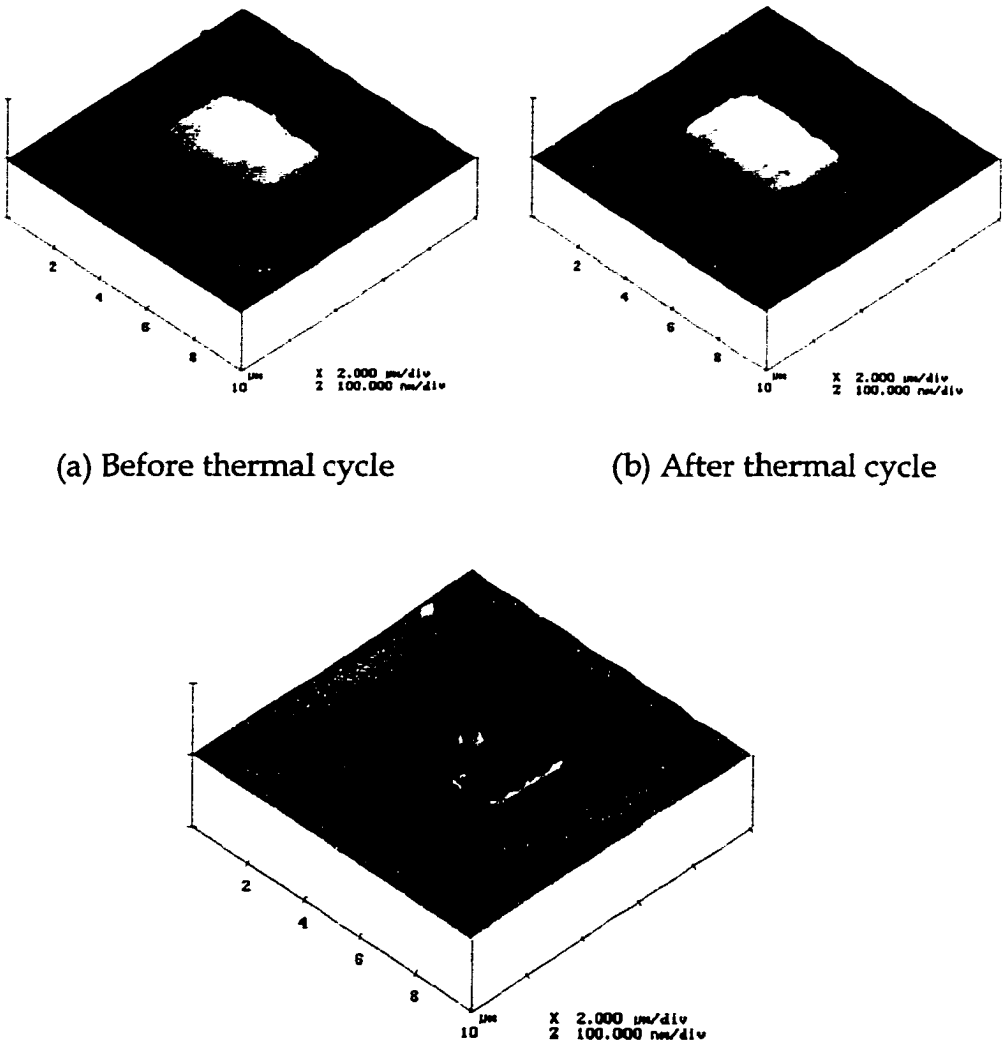
3-2 Experimental Setup

A specimen of 1 μm thick single level damascene copper-polyimide structures was fabricated by IBM using FPI-136 polyimide dielectric covered with a silicon nitride (Si_3N_4) hard mask, a tantalum diffusion barrier layer, and a proprietary copper deposition process. A small (about 1 cm x 1 cm square) test specimen was cut off the wafer for use in the thermal cycle study.

Surface topography around the areas of copper and polyimide vias were recorded at room temperature using a *Dimension 3000* atomic force microscope (AFM), operating in TappingMode™. The images were acquired at several different scan sizes to study local and larger scale deformation behavior of both areas of Cu vias in a polyimide film and polyimide vias in copper background. Then, the test specimen was heated from 25°C to 350°C at a rate of 2°C/minute in a nitrogen atmosphere, which was pre-gettered by passing it over copper fillings heated to 600 °C. The sample was then cooled back to 25°C at about the same rate. Immediately after cooling, images of surface topography of the same areas were carefully acquired using the TappingMode™ AFM, taking care to match the lateral orientation.

The topographical images obtained before the thermal cycle were then subtracted from images of the same area acquired after the thermal cycle, so that the resultant topographical images represent the out-of-plane deformation maps of the structure. The deformation maps are utilized to show evidence of high

temperature deformation mechanisms in the structure. **Fig. 3-3** illustrates an example of the image subtraction process to generate an out-of-plane deformation map of an area of copper via in polyimide background.



(a) Before thermal cycle (b) After thermal cycle

(c) Out-of-plane deformation map

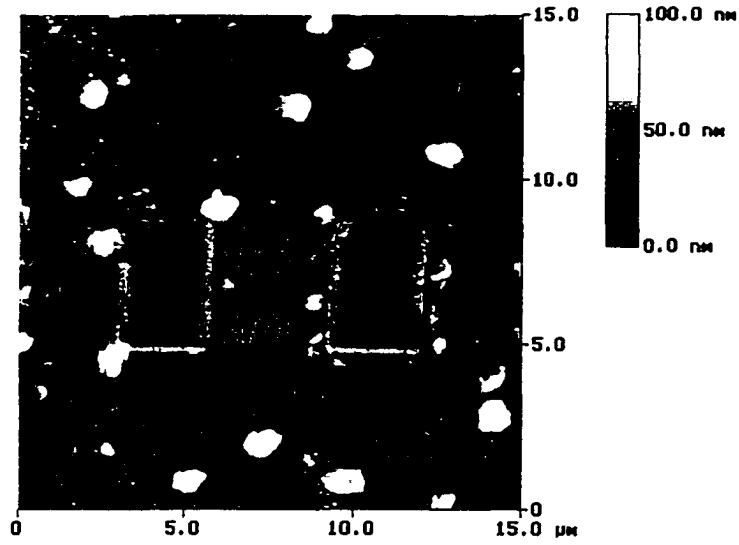
Fig. 3-3 A process of generating an out-of-plane deformation map of area of Cu via. The deformation map in (c) is obtained by subtracting the AFM image in (a) from the image in (b).

3-3 Results and Discussion

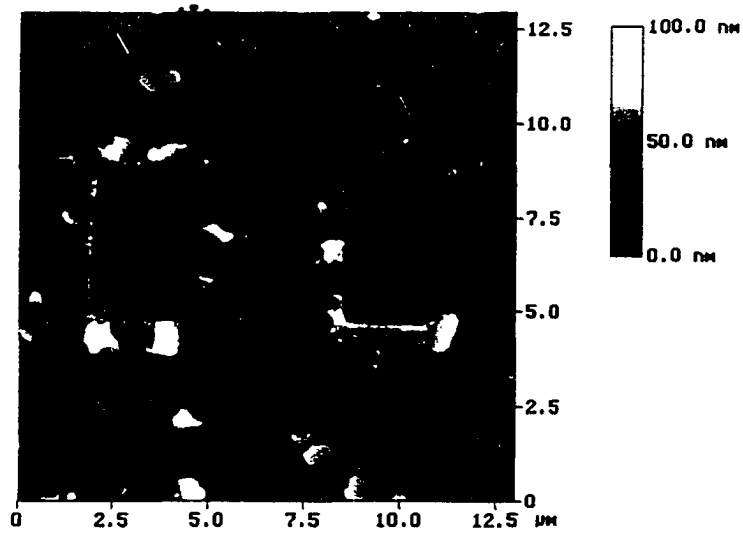
3-3-1 Heterogeneous Deformation of Copper Film

Fig. 3-4 shows out-of-plane deformation maps of copper film area surrounding a pair of polyimide vias, obtained from the same test specimen and are separated by less than 1 mm apart. One can clearly observe the differences in the surface morphology between the films. In general, the deformation map shown in *Fig. 3-4(a)* is relatively "smoother" than that shown in *Fig. 3-4(b)*. Both maps however contain what looks like large extrusions of individual copper grains at isolated areas. In *Fig. 3-4(a)* elevated Cu grains can also be seen in some areas close to the copper-tantalum interface. The elevated Cu grains are approximately 20 to 60 nm high.

Both deformation maps also contain some features that look like small voids (as enclosed within the dashed circles). Some of these features may be real voids, but some could be bits of foreign matter that were present in the AFM image obtained before the thermal cycle, but were removed after the thermal cycle. Some larger voids (as enclosed within a solid circle) can also be seen from *Fig. 3-4(a)*. In the deformation map shown in *Fig. 3-4(b)*, most of these features (as enclosed within the solid circles) are smaller grains that appear to be shrinking. **Fig. 3-5** shows plots of out-of-plane deformation profile across the polyimide vias in the deformation map shown in of *Fig. 3-4(a)*.



(a)



(b)

Fig. 3-4 Out-of-plane deformation maps of two different areas of copper film, separated by less than 1 mm apart, from the same test specimen. The obvious difference in the surface morphology demonstrates the heterogeneous nature of the film's deformation.

The Cu grains in *Fig. 3-4(a)* do not appear to have experienced any changes in relative height and the Cu grain boundaries are decorated with material that appears to have come from the grain boundaries, which is consistent with *Coble* creep deformation mechanism, in which matters diffuse through the grain boundaries to the surface of the film, in response to the in-plane biaxial compressive stresses. However, on closer examination, it appears that the grain boundary decoration consists of hemispherical features that are denser on the grain boundaries. The appearance of these features could be due to some sort of contaminant on the film's surface.

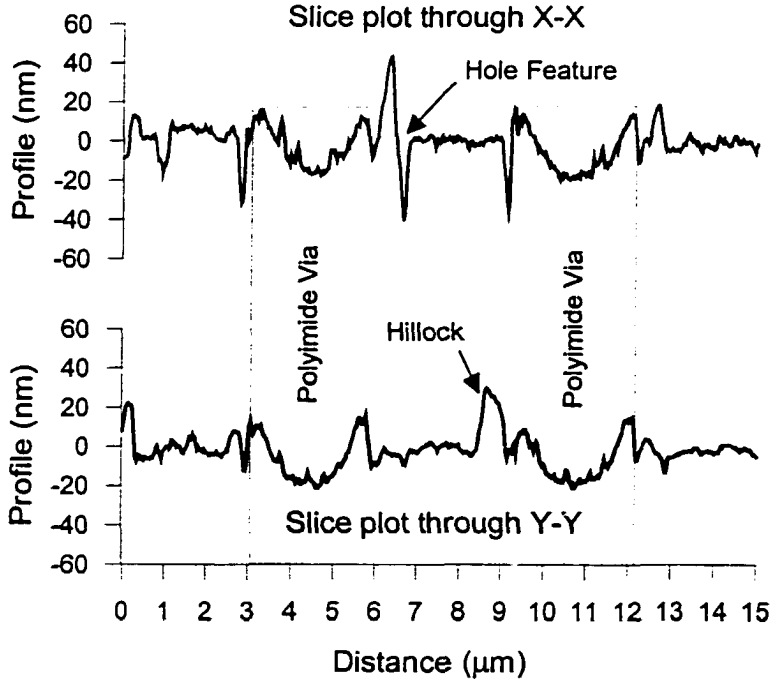


Fig. 3-5 Slice plots across the out-of-plane deformation map shown in *Fig. 3-4(a)* showing the hole feature and hillock growth in the copper film.

On the other hand, the deformation map shown in *Fig. 3-4(b)* indicates that the Cu film area experienced more deformation than that shown in *Fig. 3-4(a)*. Many of the grains in this film are elevated or depressed with respect to one another. Some of the elevated grains are tilted to a specific direction. The fact that the Cu grains appear to be elevated or depressed as a whole unit suggests that the grain boundaries are oriented at some angle to the surface normal. The grains slid up or slid down in response to the in-plane compressive stresses at elevated temperature. Large Cu grain extrusions can be seen in isolated areas near the Cu-Ta interface. Some larger and deeper hole features can be observed in this map, as shown within the solid circles. The fact that the copper film in *Fig. 3-4(b)* exhibits such an extensive deformation compared to the area shown in *Fig. 3-4(a)* demonstrates the heterogeneity of the copper film's deformation as a result of the thermal cycle.

Fig. 3-6 shows a higher resolution three-dimensional image of the out-of-plane deformation of copper film area. This deformation map shows evidence of Elevation and depression of *Coble* creep mechanism that resulted in what looks like "ditching" around the Cu grain boundary, as enclosed by the solid circle. Examples of Cu grain elevation and Cu grain depression attributed to Cu grain boundary sliding can be seen clearly in this image, as indicated. Examples of large voids can also be observed at the top right corner of the image.

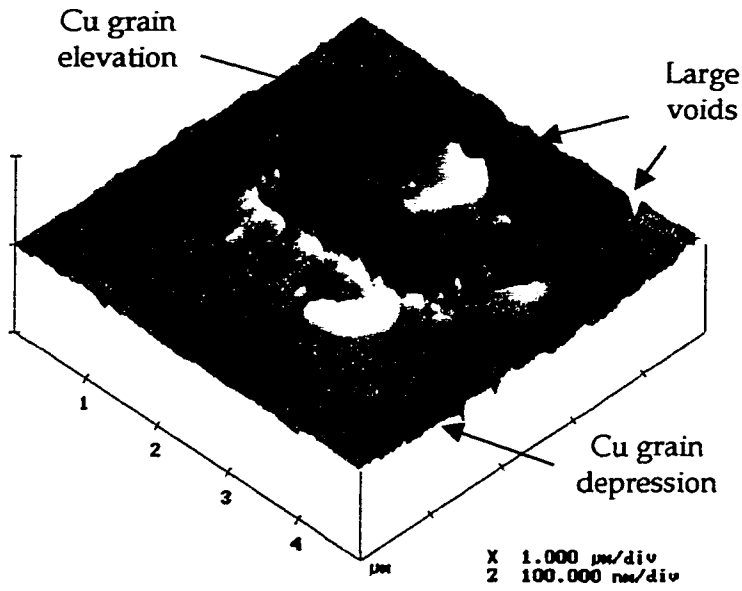


Fig. 3-6 Deformation map of Cu film area showing evidence of *Coble* creep mechanism resulting in "ditching" at Cu grain boundary as shown within the circle.

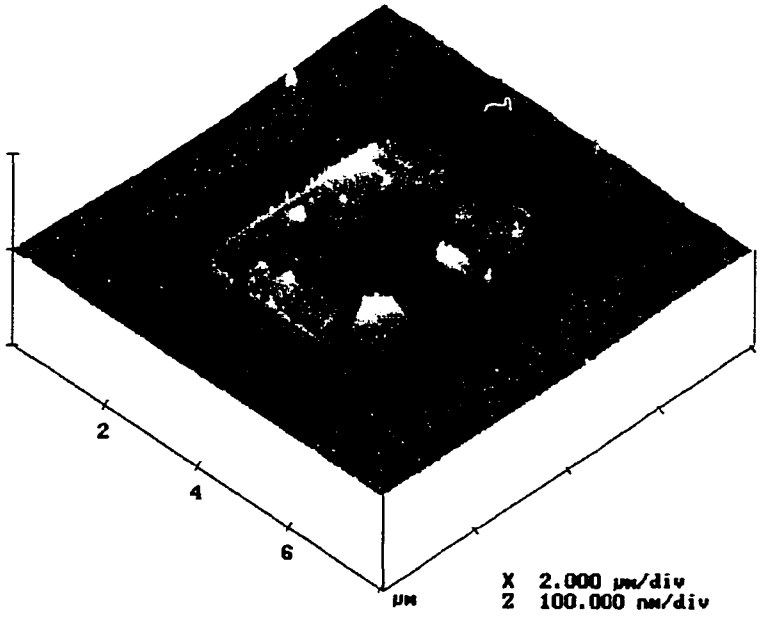
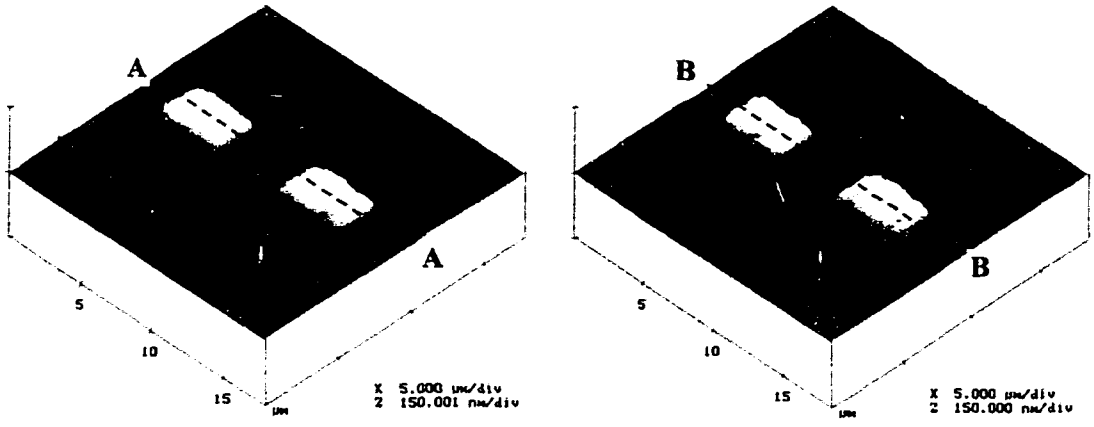


Fig. 3-7 Out-of-plane deformation map of a 3 μm x 4 μm Cu via in polyimide. Most of the copper grains near the Cu-Ta interface are elevated while the grains at the center of the via are depressed.

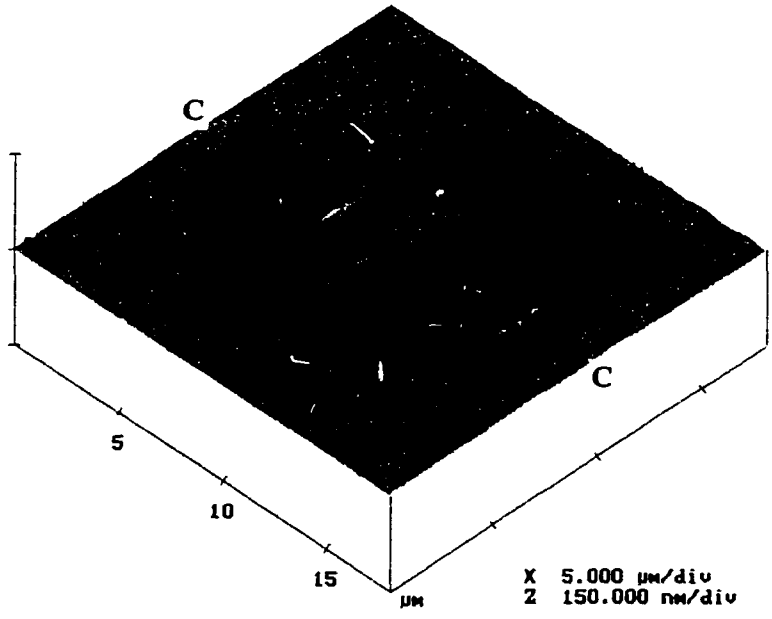
Other evidence of Cu grain boundary sliding can be seen in the deformation map of a 3 μm x 4 μm Cu via in polyimide background, shown in **Fig. 3-7**. In this image, the majority of the Cu grains on the edge of the copper via are elevated relative to the surrounding polyimide, attributed to the sliding at the Cu grain boundary, in response to the out-of-plane shear stress developed at the Cu-Ta interface at elevated the temperature. In contrast, the grains in the middle of the Cu via are depressed with respect to the surrounding polyimide.

3-3-2 Residual Deformation of Polyimide Film

Fig. 3-8 shows AFM images of surface topography of an area of polyimide film surrounding a pair copper vias. *Fig. 3-8(a)* shows the image before the thermal cycle while *Fig. 3-8(b)* shows that obtained after the thermal cycle. *Fig. 3-8(c)* shows the resulting out-of-plane deformation map of the area. It can be seen that the polyimide close to the Cu-Ta interface experienced a residual deformation as a result of the thermal cycle. The polyimide film far from the Cu-Ta interface is not expected to undergo residual deformation due to the thermal cycling [19]. The polyimide area at the left of the image is relatively smooth, indicating that the nitride hardmask does not experience residual deformation. The waviness seen on the right of the images is attributed to the buckling of the nitride hardmask during fabrication, as the structure is cooled to room temperature from polyimide curing temperature (about 350 °C), and it did not disappear after the thermal cycling.



(a) Before thermal cycle (b) After thermal cycle



(c) Out-of-plane deformation map

Fig. 3-8 Images of surface topography of polyimide film area, (a) before thermal cycle, (b) after the thermal cycle, and (c) the out-of-plane deformation map.

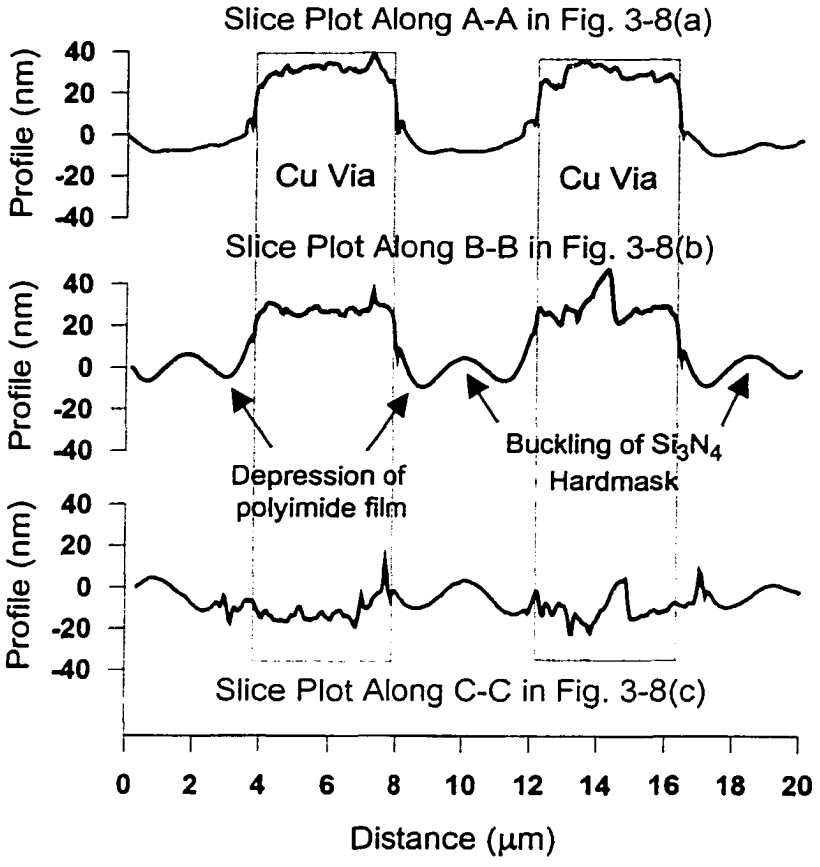


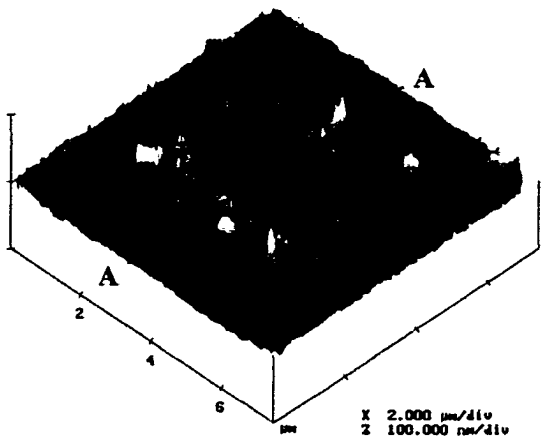
Fig. 3-9 Slice plots across the copper vias in the AFM topographical images in *Fig. 3-8(a)-(c).*

As seen from *Fig. 3-8(c),* the polyimide around the Cu vias is depressed by approximately 5-10 nm, about 1-2 μm away from the Cu-Ta-polyimide interface, as indicated by the slice plots in **Fig. 3-9**. This phenomenon is attributed to the *Poisson* contraction of the polyimide. If the Cu vias deformed due to in-plane compression during the heating and this deformation did not completely recover during the cooling cycle, then the resultant tensile stress in the polyimide would cause the film to contract normal to the film's plane. This effect would probably

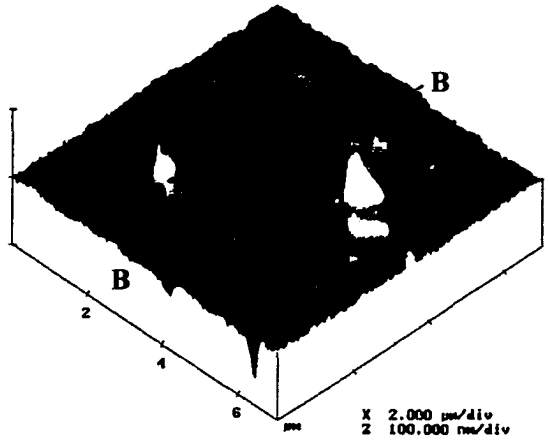
extend at least one film thickness from the interface. Closer observation on *Fig. 3-8(c)* reveals evidence of interfacial sliding at Cu-Ta interface, and this could contribute to the depression of the polyimide around the vias. However, the effect of the interfacial sliding is not expected to extend very far from the Cu-Ta interface. In fact, it appears to die off approximately 0.2 μm from the interface. The deformation map in *Fig. 3-8(c)* also shows that the polyimide between the copper vias buckles upward at the middle, by about 5-10 nm, as indicated in the slice plots of *Fig. 3-9*.

3-3-4 Interfacial Sliding at Copper-Tantalum Interface

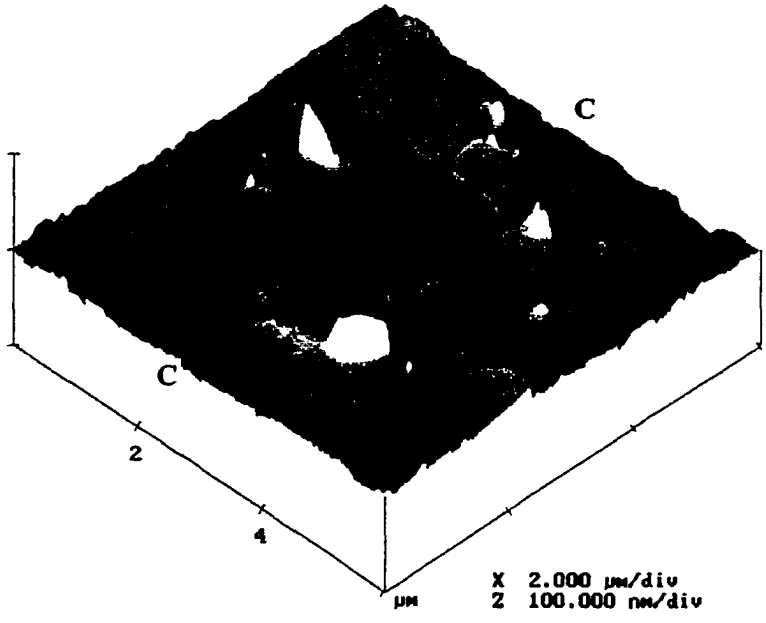
Experimental evidence of sliding at copper-tantalum interface of arrays of parallel Cu lines in damascene Cu-Ta-polyimide structure subjected to 25°C-350°C-25°C thermal cycle was reported by *Zhmurkin et.al* [20]. This phenomenon occurs because the higher CTE polyimide causes the Ta liner to slide up with respect to the Cu during the heating cycle. The sliding completely relieves the shear stress at the Cu-Ta interface, as well as deforming the Ta liner substantially elastically (and possibly plastically). As the structure was cooled back to 25 °C, the polyimide returns to its room temperature thickness, but the rate of Cu-Ta sliding is too slow to relieve the interfacial shear stress. As a result, the polyimide is "held up" at the interface. Tensile plastic deformation of the Ta liner during the heating cycle could also add to the appearance of the polyimide being held up at the interface.



(a) 3 µm x 4 µm polyimide via.



(b) 2.5 µm x 3 µm polyimide via.



(c) 2.5 µm x 2 µm polyimide via.

Fig. 3-10 Out-of-plane deformation maps of polyimide via of different sizes. Except in *Fig. (b)*, evidence of interfacial sliding at the Cu-Ta interface can be clearly seen in these images.

Fig. 3-10 shows the out-of-plane deformation of polyimide via of different sizes surrounded by copper. An evidence of interfacial sliding at the Cu-Ta interface can be seen clearly from *Fig. 3-10(a)*, resulting in the edge of the polyimide via being held up at the Cu-Ta interface, while the polyimide at the middle of the via is depressed relative to the surrounding copper. In contrast, no clear evidence of Cu-Ta sliding can be observed in the smaller polyimide via shown in *Fig. 3-10(b)*. Evidence of Cu-Ta interfacial sliding can again be seen in the much smaller via, as shown in *Fig. 3-10(c)*, but the edge of the polyimide at the Cu-Ta interface is depressed relative to the surrounding copper while the middle of the via is elevated. The above shows that the direction of Cu-Ta sliding changes from up to down as the size of the polyimide via decreases.

Fig. 3-11 shows profile plots across the polyimide via of *Fig. 3-10*. The change in the direction of the Cu-Ta sliding can be more clearly observed from these plots. The edge of the 3 μm x 4 μm polyimide via in *Fig. 3-10(a)* is elevated by approximately 15-20 nm with respect to the surrounding copper, as indicated by the plot shown at the top of *Fig. 3-11*. On the other hand, the plot shown in the middle of *Fig. 3-11* indicates that the edge of the 2.5 μm x 3 μm polyimide via in *Fig 3-10(b)* is nearly planar with the surrounding Cu film. As seen from the bottom plot in *Fig. 3-11*, the edge of the 2.5 μm x 2 μm polyimide via in *Fig. 3-10(c)* is depressed by approximately 10-20 nm with respect to the surrounding copper.

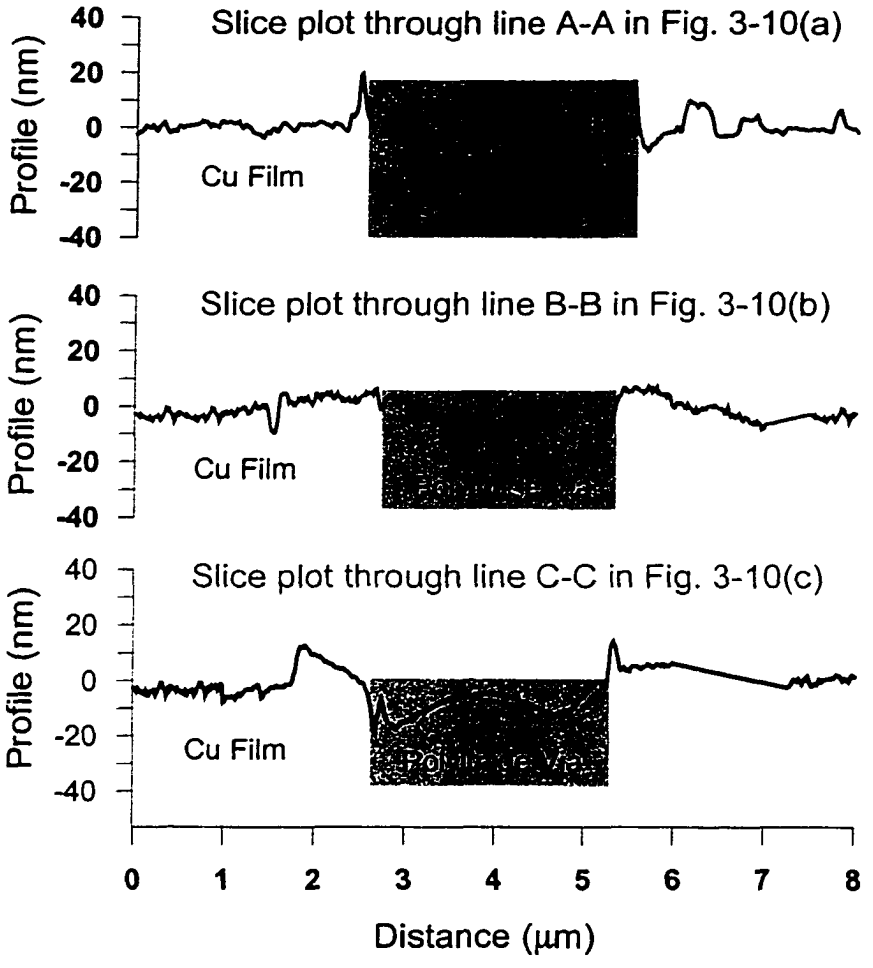


Fig. 3-11 Slice plots through the polyimide via in the out-of-plane deformation maps shown in *Fig. 3-10.*

Chapter 4 of this report describes a finite element (FE) investigation on the effects of Cu-Ta interfacial sliding in a 1 μm thick single level *Benzocyclobutane* (BCB)-Cu interconnect structure [21]. It was found that thicker Ta liner (50 nm thick) causes a downward sliding of the dielectric and the tantalum liner at the Cu-Ta interface regardless of the polymer line width, because the polymer at the interface is being constrained from the out-of-plane expansion. The FE study also

predicted that the direction of Cu-Ta sliding in the structure should change from upward to downward as the line width of the polymer dielectric decreases to the order of film thickness (about 1 μm), when the Ta liner is 10 nm thick. This is because the Ta liner becomes increasingly effective in constraining the dielectric out-of-plane expansion as the width of the BCB dielectric decreases.

Based on the above observation, one would expect a downward sliding at the Cu-Ta interface in narrower polymer structures with thin Ta liner, which is consistent with what is observed from the out-of-plane deformation maps in *Fig. 3-10(a)-(c).* Therefore, the reversal of the Cu-Ta interfacial sliding direction observed in *Fig. 3-10* can be attributed to the increasing constraint on the polyimide out-of-plane expansion as the via size decreases. The fact that the surface curvature at the center of the polyimide via changes directions as the via size decreases is also consistent with the change in the direction of Cu-Ta sliding. If the Ta liner is siding upward at the elevated temperature and did not completely reverse during the cooling cycle, then, the polyimide will be elevated at the interface with respect to the interior. On the other hand, if the polyimide at the Cu-Ta interface slides down, the center of the via will be elevated.

Other evidence of Cu-Ta interfacial sliding can also be seen in the deformation map of 3 μm x 4 μm Cu via, shown earlier in *Fig. 3-7* and in the deformation map of a 2 μm x 4 μm Cu via shown in **Fig. 3-12.** In both structures, the polyimide film is held-up at the Cu-Ta interface.

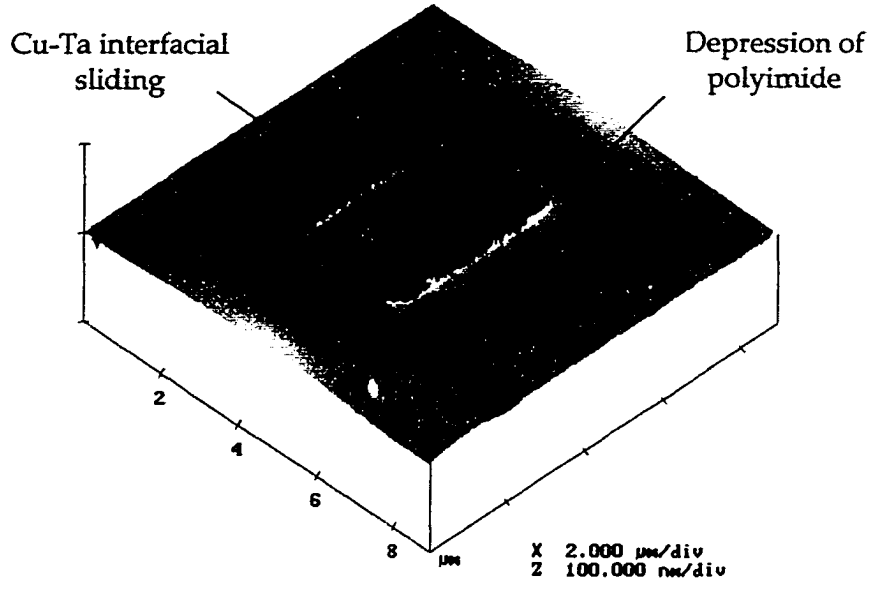


Fig. 3-12 Out-of-plane deformation map of 2 μm x 4 μm Cu via in polyimide film, showing evidence of Cu-Ta interfacial sliding and depression of the polyimide film around the via.

The depression of the polyimide around the Cu via attributed to *Poisson* contraction can also be seen in the image shown above. As mentioned earlier, the majority of the Cu grains adjacent to the Cu-Ta interface in the larger Cu via are elevated with respect to the surrounding polyimide, attributed to sliding at the Cu grain boundary. Thus, it appears that Cu-Ta sliding and Cu-Cu sliding are competing deformation mechanisms in this structure. In contrast, all the Cu grains in *Fig. 3-12* are depressed with respect to the surrounding polyimide, although evidence of Cu grain boundary sliding can also be seen. This suggests that Cu-Ta interfacial sliding is a more dominant mechanism in this structure.

It must be emphasized that the out-of-plane deformation maps shown in this section represent only the *changes* in surface topography and no fixed reference surface was used in generating these maps. It was assumed that the areas of the blanket film far away from the via structures are reasonable reference surfaces for comparing the thermal deformation of the via structures due to the thermal cycling. This is reasonable for areas of the polyimide blanket film because the film deforms only elastically due to the thermal cycling [19].

The copper films shown in *Fig. 3-4, Fig. 3-6* and *Fig. 3-10* clearly exhibit inelastic heterogeneous deformation due to the thermal cycling. Desorption of copper film surface could have occurred during the thermal cycle, which would give the impression that the copper was lower than the polyimide after the thermal cycle. However, this would have happened in a uniform manner instead of heterogeneous and microstructurally localized manner, as observed in the AFM images shown in these figures.

The image subtraction technique used to generate the out-of-plane deformation map was not a perfect procedure due to the difficulty encountered in aligning the AFM image before and after the thermal cycle. As a result, some of the deformation maps may not represent the accurate residual deformation of the structures due to the thermal cycling. The white area seen at the bottom of the polyimide vias in *Fig. 3-4(a)* is an example of this imperfection.

3-4 Summary of Deformation Mechanisms

Areas of copper film undergo a highly *heterogeneous* deformation resulting from a 25°C-350°C-25°C thermal cycle. The out-of-plane deformation maps of the Cu film exhibited evidence of:

a) Sliding at Cu grain boundary, resulting in extrusion of large individual Cu grains in isolated areas, elevation and depression of smaller Cu grains, which are tilted to a specific direction.

b) *Coble* creep mechanism, producing what looks like "ditching" around the Cu gain boundary.

c) Formation of small and larger voids.

d) Shrinking of smaller Cu grains.

In addition to these classical high temperature deformation mechanisms, evidence of interfacial sliding at Cu-Ta interface was also observed in both areas of copper and polyimide via structure, resulting in the edge of the polyimide being held-up at the interface. In the larger Cu via, Cu-Ta sliding and Cu grain boundary sliding appear to be competing deformation mechanisms, while in the smaller via structure, Cu-Ta sliding seems to be a more dominant mechanism. The direction of the Cu-Ta sliding changes as the size of the polyimide via decreases, attributed to increasing constraint on the out-of-plain expansion of the polyimide.

The polyimide around the copper via experienced depression due to *Poisson* contraction, attributed to in-plane deformation of the Cu via and interfacial sliding at the Cu-Ta interface.

Chapter 4

FINITE ELEMENT MODELING OF THE EFFECTS OF Cu-Ta INTERFACIAL SLIDING IN COPPER INTERCONNECT STRUCTURES

4-1 Stress Development and Relaxation

Thermal stresses are developed in copper interconnect structures owing to the large difference in the *coefficient of thermal expansion* (CTE) between the silicon substrate, dielectric material, Ta liner and copper conductor, and the difference between room temperature and elevated dielectric deposition temperature, encountered during the fabrication process. The oxide dielectric is typically deposited at about 350 °C. When the structure is cooled back to room temperature, copper contracts more than the thick silicon substrate and is therefore subjected to biaxial tension, greater that its yield strength. In a continuous copper film, plastic deformation allows the film to shrink in thickness to accommodate the stresses, as its lateral dimensions are constrained to match those of the silicon.

Fig. 4-1 shows a schematic of parallel copper interconnect wires encased in SiO_2 dielectric, as typically found in real integrated circuit (IC) microchips. Assuming that the copper lines adheres to the surrounding SiO_2, as the structure cools from the dielectric deposition temperature to room temperature, the higher CTE copper is brought into hydrostatic tension. In this case the Cu wires do not

have the "thickness" degree of freedom as in the continuous film, with which plastic deformation can accommodate tension in the other two directions. If the hydrostatic tension is greater than the cavitation stress for copper, it can only be accommodated by the formation of voids. The void volume may be in the order of 1% of that of copper, an insignificant fraction if the size of the voids is in the order of *nanometers*. However, if these voids coalesce into a few large voids, they can produce a complete breakage of the metal wires, resulting in failure of the structure [22].

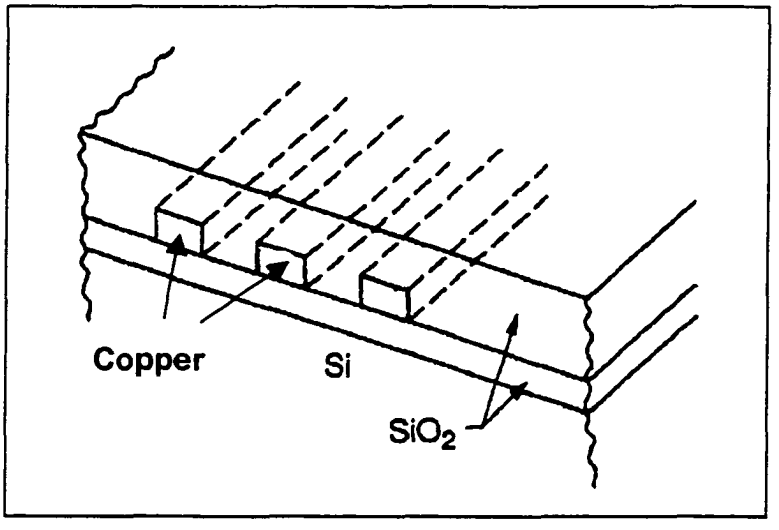


Fig. 4-1 A schematic illustration of Cu wires confined on all sides by SiO_2 dielectric. The wires are brought into hydrostatic tension during cooling from the SiO_2 deposition temperature.

4-2 Stress-Temperature Behavior in Copper Film

Thermal stresses developed stresses in the Cu interconnect structures due to CTE mismatch can have a severe impact on the processing and reliability of

the interconnection structures. To quantify the effects of these stresses, one need to incorporate an understanding of the relaxation mechanisms that are appropriate for the material components under the condition of interest. One approach used by many researchers to investigate these mechanisms is to measure the development of stresses during a thermal cycling of a metal film deposited on a substrate. The temperature dependence of stresses in copper blanket films has been measured and modeled by *Flinn et.al* [23]. **Fig. 4-2** shows a stress-temperature *loop* measured in 1 μm thick sputtered copper film subjected to a 600 °C thermal cycle.

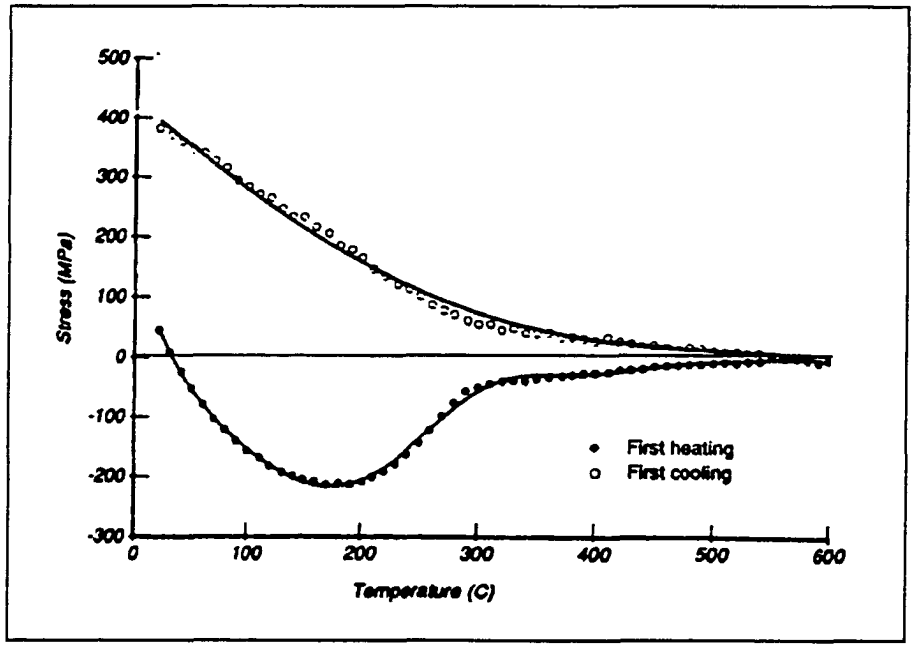


Fig. 4-2 A stress-temperature *loop* for 1 μm thick blanket copper film on silicon, subjected to a 600 °C thermal cycle, produced by wafer curvature technique. (Adapted from [23]).

The small tensile stress initially present in the film is a result of cooling after the film deposition. On heating, the elastic strain due to the difference in CTE between the copper and the silicon results in a linear decrease in the stress-temperature curve. The stress changes sign from tensile to compressive at temperatures below 100 °C. On further heating, the stress becomes large enough to cause plastic deformation in the film and stress increases less rapidly with increasing temperature. In the temperature range of 200 °C to 300 °C, there is a rapid drop in the compressive stress in the film, attributed to *recrystallization* of copper [24]. The stress remains low during the rest of the heating cycle, and becomes essentially zero at 600 °C. During the cooling cycle, copper contracts more rapidly than the silicon substrate, resulting in the development of tensile stress in the film. However, much of the tensile stress is accommodated by plastic deformation of the structure.

A numerical modeling of stress development and relaxation in 1 μm thick Cu films during thermal cycling to elevated temperatures in the range of 25°C to 450°C was reported by *Thouless et.al* [25]. The results were portrayed on deformation mechanisms maps of *Frost and Ashby* [26] that identify the dominant mechanisms expected to operate during the thermal cycling. It was shown that grain boundary diffusion (or *Coble* creep) controls the stress relief at high temperatures (above 300 °C), when only low stresses can be sustained in the films. *Power-law* creep is important at intermediate temperatures and low-

temperature plasticity (yield by dislocation glide) can only occur at temperatures lower than 100 °C. It was also demonstrated that stress relaxation in Cu blanket film could be adequately modeled by applying the creep properties of bulk polycrystalline copper to the thin Cu films.

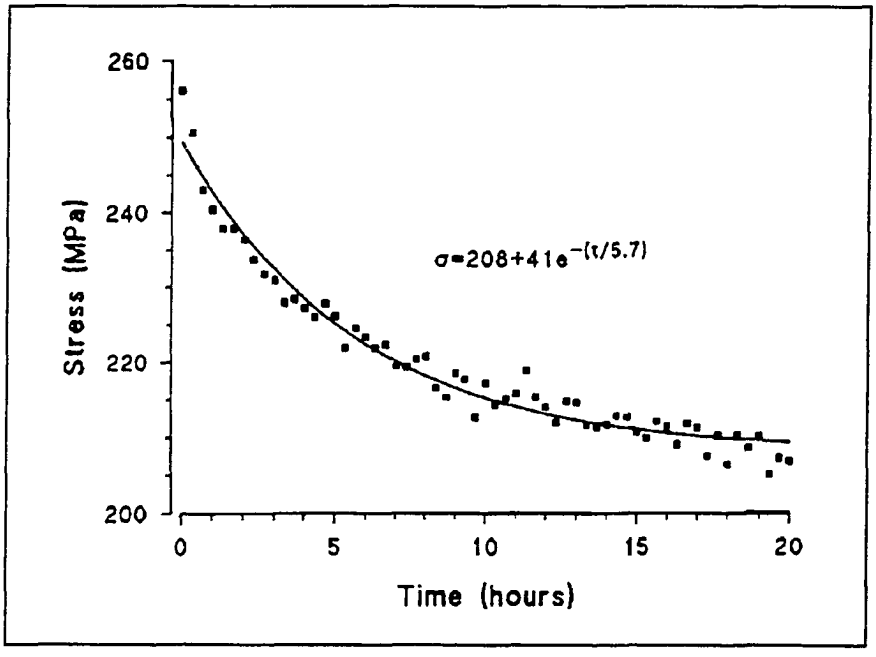


Fig. 4-3 Stress relaxation in Al-Si-Cu film held at 70 °C, after cooling from 400 °C. The stress data fits exceptionally well to an exponential function in the form of $\sigma = A + Be^{-(t/t)}$. (Adapted from [27]).

Stress relaxation in 1 μm thick Al-Si-Cu film deposited on oxidized silicon subjected to a thermal cycle to 400 °C was described by *Draper et.al* [27]. They demonstrated that if the temperature is paused during the cooling part of the cycle, the stress in the film would relax with time, following a trend shown in **Fig. 4-3**. The stress data fits an exponential function in the form [27]

$$\sigma = A + B \cdot e^{-\left(\frac{t}{\tau}\right)} \qquad (4\text{-}1)$$

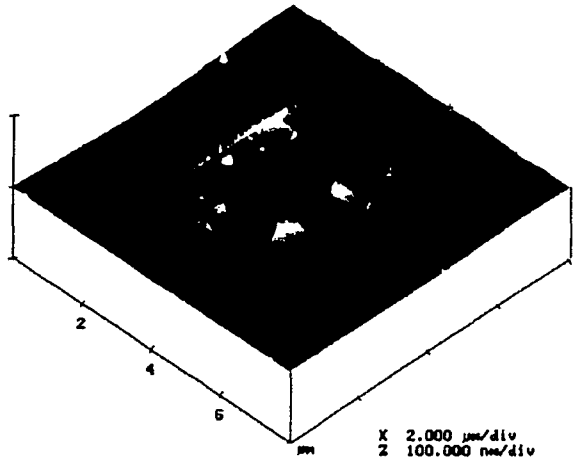
where σ is the stress, A and B are constants, t is the holding time, and τ is a *relaxation time* constant, a parameter that can be used to compare stress relaxation rate in various films. The value of τ is small at smaller grain size and it increases linearly with increasing grain size.

4-3 Stress Relaxation in Interconnect Structure

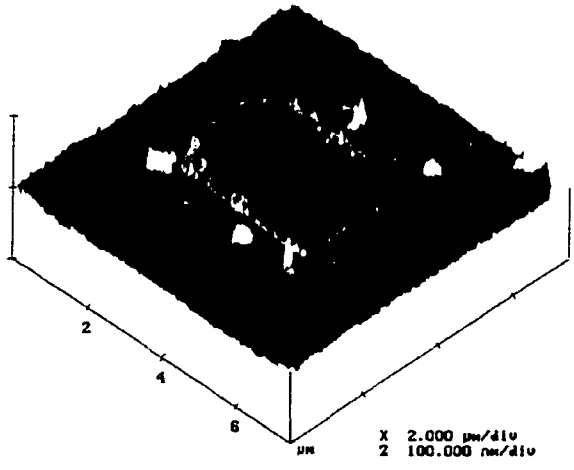
During fabrication process of multilevel copper interconnection structures, the existing wiring layers may be subjected to several thermal cycles up to 350 °C. Thermal stresses develop in the structures owing to mismatch in both in-plane and out-of-plane coefficient of thermal expansion (CTE) between the silicon substrate, dielectric material, tantalum liner and copper. As the existing interconnection layers are heated to the peak processing temperature, copper experiences significantly high homologous temperature (about 0.45 T/T_m, where T_m is the melting temperature of copper). This allows *diffusion-accommodated interfacial sliding* (interfacial creep) to operate at the Cu-Ta vertical interface to relax the interfacial shear stresses in the structure [12].

Experimental evidence of *diffusion-accommodated* Cu-Ta sliding was observed in the AFM investigation of thermally induced inelastic deformation of Cu and polyimide via areas in a single level Cu-polyimide interconnect structure

subjected to a 25°C-350°C-25°C thermal cycle, described earlier in *Chapter* 2 of this report. **Fig. 4-4** show examples of the Cu-Ta interfacial sliding phenomena in copper and polyimide via areas.



(a)



(b)

Fig. 4-4 Out-of-plane deformation maps of (a) area of 3 x 4 µm Cu via and (b) area of 3 x 4 µm polyimide via structure resulting from a 25°C-350°C-25 °C thermal cycle. Both maps exhibit evidence of interfacial sliding at the Cu-Ta interface resulting in the edge of the polyimide being held-up at the interface.

4-4 Effect of Cu-Ta Sliding on Stresses

Zhmurkin [10] has investigated the effects of Cu-Ta interfacial sliding on the stresses at parallel Cu lines structure in a single level copper-polyimide interconnect structure using a finite element method (FEM). The Cu-Ta sliding effect was produced using a 1 nm thick sliding element incorporated into the finite element models between copper and tantalum liner. The sliding element, having elastic material properties similar to copper, was calibrated so that the steady-state creep strain rate matches the prediction of analytical sliding model proposed by *Raj and Ashby* [13]. It was shown that the sliding caused the out-of-plane shear stress at the interface to relax in exponential decay with time and the rate of stress relaxation is a strong function of temperature.

In this study, a similar finite element study was carried out to simulate Cu-Ta interfacial sliding at parallel lines arrays in 1 μm thick single-level *Benzocyclobutane* (BCB)-copper and SiO_2-copper interconnect structures, as a result of heating from 20 °C to 400 °C, assuming that the structures are stress free at 20 °C. The goals are to estimate the thermal stresses developed in the structures at 400 °C and to predict the effects of the sliding on the interfacial and liner plane stresses. The effect of the Cu-Ta sliding on the stresses was evaluated by comparing the stresses in *relaxed* and *unrelaxed* states. The Cu-Ta sliding effect was produced using a 1 nm thick sliding element and the previously used interfacial sliding model was adopted. The effects of line *width-to-thickness* (*w/t*)

ratio and Ta liner thickness on the stresses at the dielectric-Ta interface and the liner plane stress in the tantalum were also investigated because these are possible sites of stress-induced failure in the structures.

Sliding at Cu-Ta interface for parallel Cu line arrays in copper-polyimide interconnect structure subjected to thermal cycle to 350 °C was reported by *Zhmurkin et.al* [28]. It was shown that little or no sliding was observed at the Cu-Ta interface for 10 μm wide Cu lines because Cu grain boundary sliding provides an alternative path for the relaxation interfacial shear stresses. In this study, the effect of Cu grain boundary sliding on the Cu-Ta interfacial sliding and relaxation of out-of-plane interfacial shear stress at dielectric-Ta interface in a BCB-Cu system having *width-to-thickness* aspect ratio 20 and 10 nm thick Ta liner was also investigated. The Cu grain boundary sliding effect was produced using the same sliding element used for modeling the Cu-Ta sliding, except that the steady-sate sliding rate is twice as fast.

4-5 Analytical Model of Interfacial Sliding

Raj & Ashby [13] have modeled interfacial sliding at grain boundaries of various shapes and proposed that at high temperatures, the stresses that are developed at a non-planar boundary could set up a diffusive flux of matter from the compressed part of the boundary to the part in tension. This results in a *steady state* diffusion-controlled interfacial sliding at the boundaries. For a *sinusoidal* or *periodic* interface boundary with wavelength λ and amplitude $h/2$

illustrated schematically in **Fig. 4-5**, the steady state sliding rate is given by the expression [13]

$$\dot{U} = \frac{8}{\pi} \cdot \frac{\tau_a \cdot \Omega}{kT} \cdot \frac{\lambda}{h^2} \cdot D_v \cdot \left\{ 1 + \frac{\pi\delta}{\lambda} \cdot \frac{D_b}{D_v} \right\} \qquad (4\text{-}2)$$

where, τ_a is a uniform shear stress applied to the boundary, Ω is atomic volume, h is total height of the boundary shape, δ is thickness of the boundary diffusion path, D_v is lattice diffusion coefficient, D_b is grain boundary diffusion coefficient, k is *Boltzmann's* constant and T is the absolute temperature.

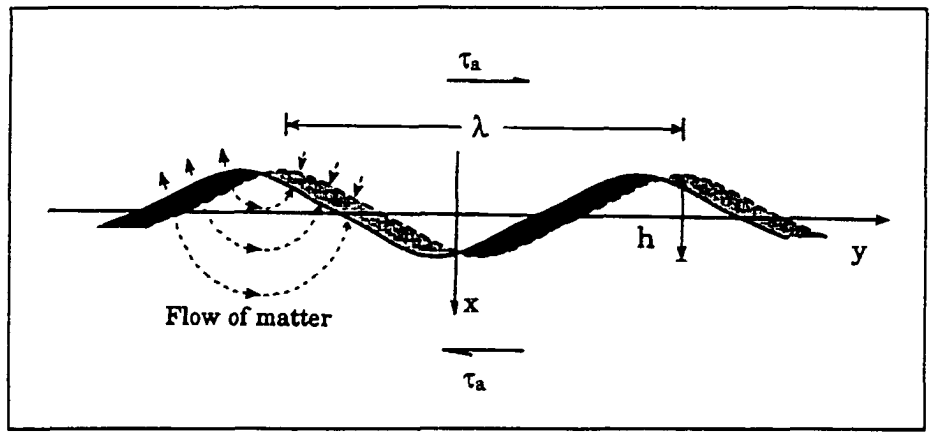


Fig. 4-5 A schematic illustration of a steady state diffusion-accommodated interfacial sliding at a *sinusoidal* grain boundary proposed by *Raj & Ashby*. (Adapted from [13]).

During the steady state sliding, vacancies are neither created nor destroyed within the two adjoining grains or crystals, which means that the boundary between them is the only source or sink for the vacancies. The term $\{(\pi\delta/\lambda)\cdot(D_b/D_v)\}$ on the right of *Eq. (4-2)* represents a dimensionless quantity. If it is large compared to unity, the transport is mainly by *boundary diffusion*, and the

sliding rate becomes independent of the wavelength λ, but depends only on the amplitude as $1/h^2$. When the term is small compared to unity, *lattice* or *volume diffusion* becomes dominant, in which the sliding rate varies as λ/h^2. In general, a short wavelength and a low temperature favor transport by boundary diffusion, whereas a long wavelength and a high temperature favor volume diffusion. For a given value of $\{(\pi\delta/\lambda)\cdot(D_b/D_v)\}$, the sliding rate decreases rapidly as the boundary becomes increasingly *non-planar*.

4-6 Finite Element Implementation

Fig. 4-6 illustrate schematically a typical construction of a single level copper interconnect structure, comprising a thick silicon substrate, dielectric material, copper and thin tantalum liner used as a diffusion barrier layer. Shown at the bottom of the figure is a representative section used as a basis for constructing the finite element model of the structures. This section was chosen based on periodicity and symmetry of the structure. The mechanical boundary conditions prescribed to the finite element models are also shown in the figure. The entire left side is constrained from displacement in x-direction, but is allowed to experience displacement in the y-direction. An x-displacement equal to the elastic expansion of the Si substrate is prescribed to the entire right side of the model. The base of the finite element model is fixed in the y-direction but is allowed to be displaced in the x-direction.

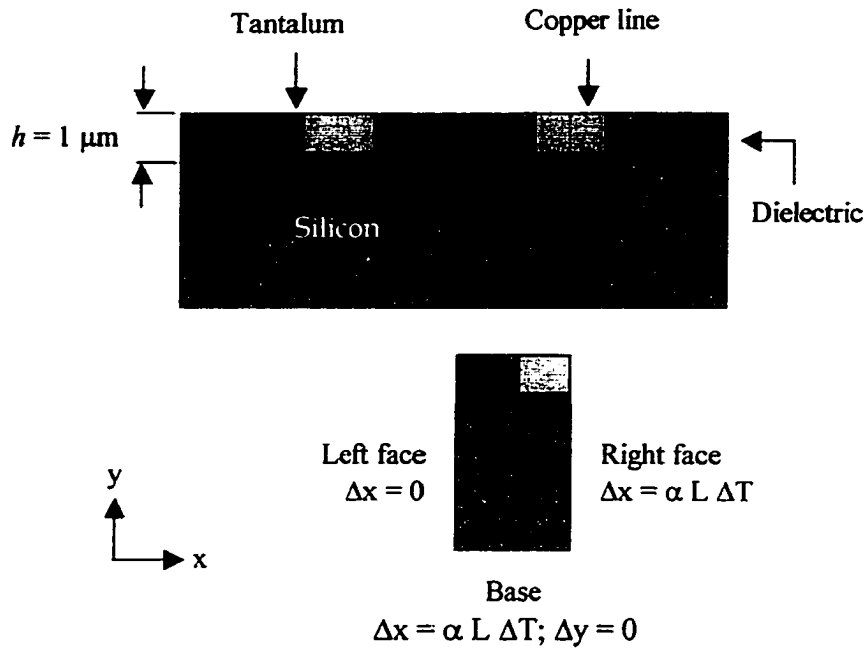


Fig. 4-6 A schematic illustrating a typical construction of a parallel copper line structure in 1 μm thick *damascene* copper interconnect structure. A representative section used as the basis for constructing the finite element models is shown at the bottom.

4-6-1 Assumptions

The following assumptions were made to simplify the construction of the finite element models and the simulation of the Cu-Ta sliding:

a) The copper-dielectric interconnect structure has a simple geometry, in which all surfaces are perfectly planar, and all interfaces are perfectly straight.

b) All material components are homogeneous, isotropic and linear elastic, and are bonded perfectly at common interfaces and at film-substrate interface.

c) The Ta-Cu sliding occurs only at peak temperature of 400 °C. Stress relaxation during the heating period was not considered, although in real structures, the Cu-Ta sliding may also occur during the heating period.

d) The Cu-Ta interfacial sliding takes place *in* the 1 nm thick sliding element, and not through the boundary *between* the Cu and Ta. Thus, continuity of strain at the Cu-Ta interface is maintained during the entire analysis.

e) The structures are in a state of zero stresses at 20 °C, and the stresses develop gradually as temperature is increased.

4-6-2 Construction of Finite Element Models

Finite element (FE) models of parallel copper lines structure were constructed using isoparametric 4-node quadrilateral plane-strain elements, based on the representative section shown at the bottom of **Fig. 4-6**. A 1 nm thick creep element was incorporated into the finite element models to produce the Cu-Ta sliding effects in the structures at 400 °C. The thickness of the element was chosen to represents a typical thickness of copper grain boundary, which is approximately in the order of three to four *Burgers* vector. The *Burgers* vector for copper is 2.56×10^{-10} m [26].

The finite element simulations were performed using commercial MARC/Mentat finite element software. The standard software package was enhanced by incorporating a user-defined subroutine of the analytical diffusion-accommodated sliding model of *Raj & Ashby* [13], adopted in the sliding simulation. Various line width-to-thickness (*w/t*) ratio and Ta thicknesses were considered in the analysis to evaluate the effects of structural geometry on stresses. These are shown in **Table 4-1** below. Hereafter, *w* denotes the width of the conductor line and *t* is the thickness of the film.

Table 4-1 The width-to-thickness (*w/t*) ratio and Ta thickness of the BCB-Cu and SiO_2-Cu interconnect systems evaluated in this study.

Width-to-thickness (*w/t*) ratio	Ta thickness (nm)	
0.2	10	-
1	10	50
20	10	-

Fig. 4-7(a) shows the finite element meshing of the SiO_2-Cu system and **Fig. 4-7(b)** shows the meshing of the BCB-Cu system, both having *w/t* aspect ratio 1 and 10 nm thick Ta liner. The film, comprising the dielectric, Ta liner, and copper, is 1 μm thick. The 1 nm thick sliding element (colored light brown) is shown in the smaller image at the top of *Fig. 4-7(b)*. The top surface of the BCB dielectric in *Fig. 4-7(b)* is covered by a 100 nm thick silicon nitride (Si_3N_4) layer,

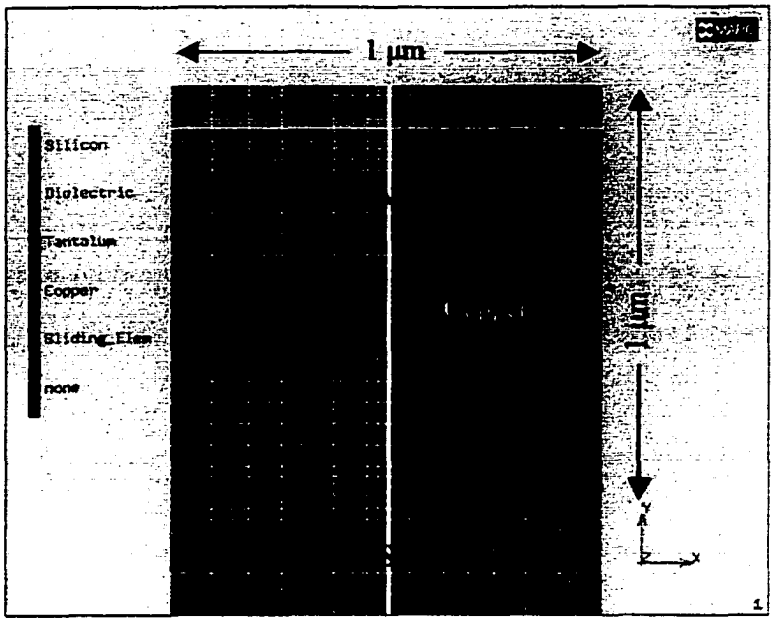
which is used as a polishing stop in the planarization step during fabrication. The top surface of the SiO_2 dielectric is completely exposed. A 1 μm thick silicon substrate was incorporated into the finite element models so that a more realistic boundary condition is prescribed at the film-substrate interface. In a real structure however, the silicon substrate is several times thicker than the film, but preliminary simulations have shown that at a depth of 1 μm from the film-substrate interface, the stresses in the substrate become negligibly small, so that there is no need to model the rest of the silicon substrate.

The thick silicon dictates the lateral expansion of the film. When the temperature is raised from 20 °C to 400 °C, the substrate expands elastically in lateral direction, by an amount Δx_{Si}, given by:

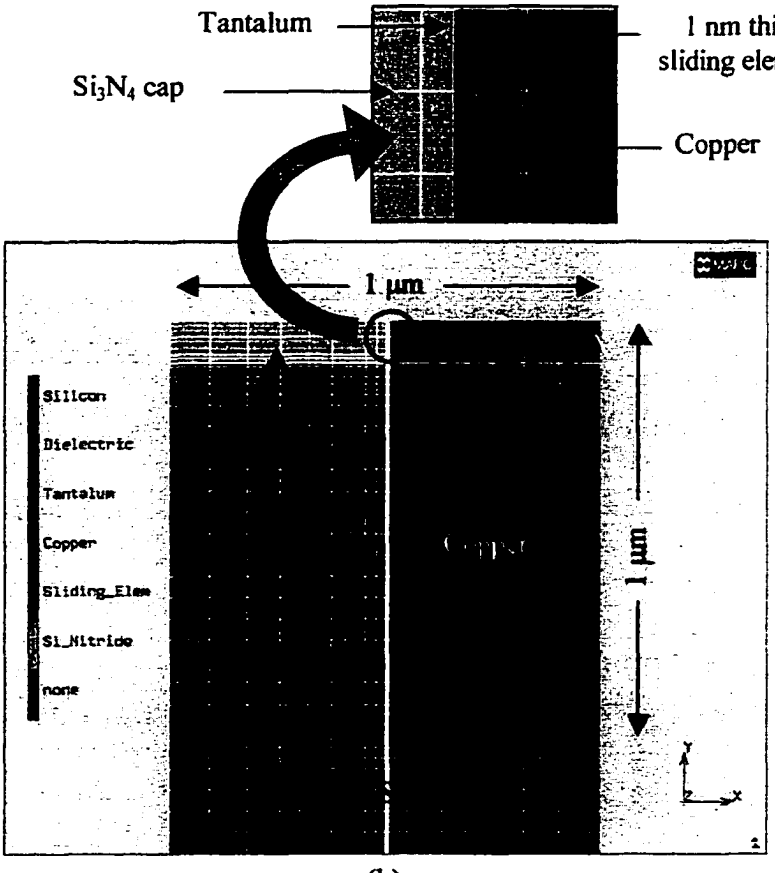
$$\Delta x_{Si} = \alpha_{Si} \quad w \quad \Delta T \qquad (4\text{-}3)$$

where α_{Si} is the coefficient of thermal expansion (CTE) of the Si substrate, w is the entire width of the models, and ΔT is the temperature change. The lateral displacement given by *Eq. (4-3)* was applied to the entire right edge of the models, with no constraint in vertical direction.

As stated earlier, except for the sliding creep element, all material components in both systems were assumed homogeneous, linear elastic and isotropic. Elastic modulus, E, *Poisson* ratio, v, mass density, ρ, and coefficient of thermal expansion, α, were prescribed to all the material components.



(a)



(b)

Fig-4-7 Finite element mesh of (a) SiO_2-Cu structure, (b) BCB-Cu structure. The *w/t* ratio is 1 and Ta liner is 10 nm thick.

The elastic properties of the sliding element were assumed the same as those for copper. In retrospect, this may introduce a slight error in the stresses, but it should be small due to the size of the element. The mechanical properties of all the materials are shown in **Table 4-2**. The analytical model of *diffusion-accommodated* interfacial sliding of *Raj & Ashby* [13] was adopted to produce the sliding effect at the Cu-Ta interface. The steady-state sliding rate is given by

$$\dot{\gamma} = \frac{8}{\pi} \cdot \frac{\tau_a \Omega}{kT} \cdot \frac{1}{h^3} \cdot \left\{ \lambda D_{ov} \exp(-\frac{Q_v}{kT}) + \pi \delta D_{ob} \exp(-\frac{Q_b}{kT}) \right\} \qquad (4\text{-}4)$$

where τ_a is the applied constant shear stress, h is height of the boundary shape, Ω is atomic volume, δ is thickness of the grain boundary diffusion path, λ is wavelength of the roughness of the grain boundary, k is *Boltzmann's* constant, T is absolute temperature, D_{ov} and D_{ob} are pre-exponential constants, Q_v and Q_b are activation energies for *lattice* and *boundary* diffusion, respectively. The value of these parameters is given in **Table 4-3**, with h and λ both equal to 1 nm.

4-6-3 Simulation of the Cu-Ta Sliding

The FE simulation of the Ta-Cu interfacial sliding was carried out using MARC/Mentat finite element software in two steps. First, a linear elastic plane strain analysis was carried out, in which temperature was gradually raised from 20°C to 400°C. Immediately after that, creep analysis was performed, in which temperature was held constant at 400 °C to allow the steady-state sliding effect to occur at the Cu-Ta interface. The finite element simulation was terminated when

the shear stress at a representative node at the interface has relaxed to a negligibly small value.

Table 4-2 The elastic mechanical properties of material components adopted in the finite element models of the BCB-Cu and SiO_2-Cu interconnect systems.

Material	Elastic Modulus, (GPa)	Poisson's Ratio ν	CTE, (10^{-6}/K)
Benzocyclobutane (BCB)	2	0.30	52.0
Copper (Cu)	128	0.36	16.5
Silicon Dioxide (SiO_2)	66	0.25	2.5
Silicon Nitride (Si_3N_4)	158	0.26	3.0
Sliding element (creep)	128	0.36	16.5
Tantalum (Ta)	186	0.34	6.5
Silicon (Si)	165	0.22	2.3

Table 4-3 Value of the parameters appearing in *Eq. (4-4)*, for copper (Adapted from [26]).

Parameter in Eq. (4-4)	Value
Atomic volume, Ω ($m^3/atom$)	1.18×10^{-29}
Boltzmann's constant, k ($J/K\ atom$)	1.381×10^{-23}
Pre-exponential, D_{ov} (m^2/s)	2.0×10^{-5}
Activation energy, Q_v ($kJ/mole$)	197
Pre-exponential, δD_{ob} (m^3/s)	5.0×10^{-15}
Activation energy, Q_b ($kJ/mole$)	104

It must be emphasized that the steady state sliding rate given by *Eq. (4-4)* applies only to interface boundary between two identical materials, in which both sides of the interface contribute to the sliding at the elevated temperature. It is proposed in this study that only copper atoms are involved in the Cu-Ta sliding because the peak temperature involved in this investigation (400 °C) is far too low for substantial lattice diffusion to occur in the Ta liner (the melting temperature of tantalum is about 3000 °C as opposed to 1083 °C for copper). For this reason, a multiplication factor of 0.5 is introduced into the expression of the steady state sliding rate in *Eq. (4-4)*.

4-7 Results and Discussion

As the temperature is raised from a 20 °C to 400 °C during the finite element simulation, stresses are gradually developed in the structure due to the mismatch in the in-plane and out-of-plane CTE between the material components in the structure. In the following sections, the effects of width-to-thickness (*w/t*) aspect ratio, Ta liner thickness, and Cu-Ta sliding on the interfacial and liner plane stresses in both systems are discussed. The effects of Cu-Ta sliding on the stresses are evaluated by comparing the stresses in the *unrelaxed* and *relaxed* states. Finally, the effect of Cu grain boundary sliding on Cu-Ta sliding and relaxation of shear stress at dielectric-Ta interface in BCB-Cu structure with *w/t* ratio 20 and Ta thickness 10 nm is discussed.

4-7-1 Effects of Width-to-Thickness (w/t) Ratio on Stresses

Fig. 4-8 shows the effect of width-to-thickness (*w/t*) aspect ratio on the out-of-plane shear stress at dielectric-Ta interface in both BCB-Cu and SiO_2-Cu systems with 10 nm thick Ta liner. The results for the corner nodes are not accurate due to the errors introduced by the finite element discretization and are therefore not included in the plots.

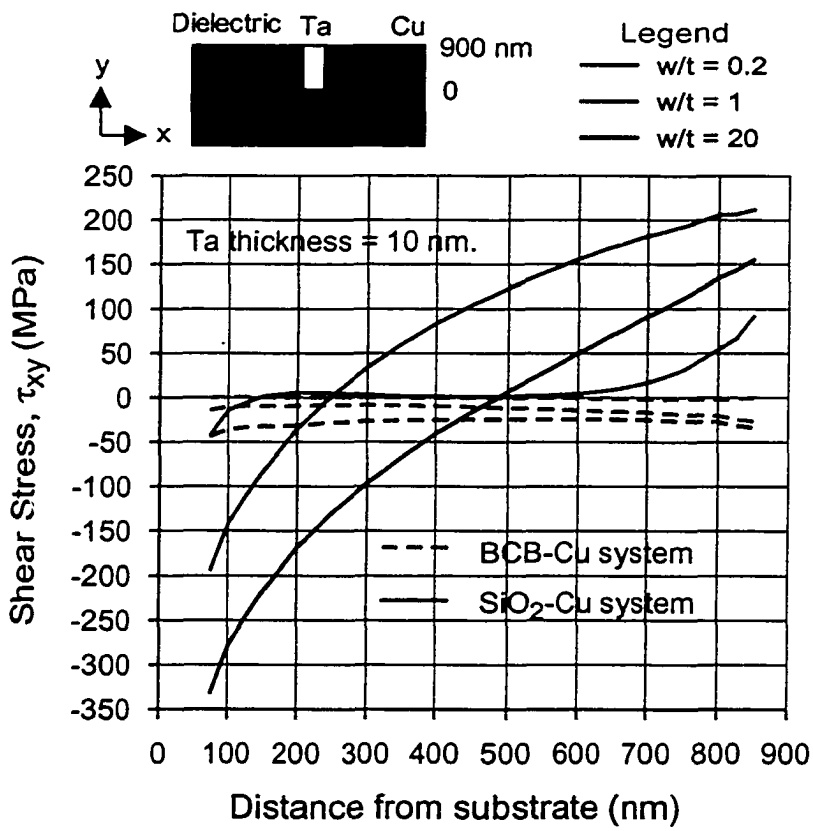


Fig. 4-8 The effect of *w/t* ratio on dielectric-Ta out-of-plane shear stress in the BCB-Cu and SiO_2-Cu systems with 10 nm thick Ta liners.

It can be seen that, when the *w/t* ratio is *0.2* the BCB dielectric is constrained from out-of-plane expansion by the nitride (Si_3N_4) cap, the adjacent

copper, and the Ta liner. The shear stress at the BCB-Ta interface is less than -3 MPa. When the *w/t* ratio is increased to *1*, the BCB dielectric becomes less constrained from expanding, and the BCB-Ta shear stress increases (becomes more negative) to a modest value of 10-20 MPa. When the *w/t* ratio is 20, the stress on the interface increases further by 30-40 MPa, which is still a low shear stress. For *w/t* ratio of 0.2, the shear stress at the SiO_2-Ta interface in the SiO_2-Cu system varies from -40 MPa near the bottom to 90 MPa near the top of the interface. As the *w/t* ratio is increased to 1, the shear stress near the top and bottom of the SiO_2-Ta interface increases in magnitude to about ± 200 MPa. When the ratio is further increased to 20, the shear stress near the top and bottom of the interface increases to 150 MPa and -300 MPa respectively. These are significant shear stresses and could affect the interfacial shear strength.

The Ta liner is subjected to an axial stress normal to the plane of the film as temperature is raised from 20 °C to 400 °C. The stress plots in **Fig. 4-9** shows the effect of *w/t* ratio on the Ta liner-plane stress in both systems when the Ta liner is 10 nm thick. When the *w/t* ratio is 0.2, the Ta liner stress in the BCB-Cu system is at its lowest value of about 1.1 GPa. The stress near the top and bottom of the Ta is about 200 MPa higher due to the effect of stress concentration at sharp corners. When the ratio is increased to 1, the Ta stress increases in magnitude to 1.6-2.0 GPa. The Ta liner stress is approximately 2 GPa at the top but decreases to less than 1 GPa near the bottom when the *w/t* ratio is 20. The Ta

liner-plane stress in the SiO_2-Cu system is about 600 MPa when the *w/t* ratio is 0.2 and it increases to 800 MPa near the bottom when the ratio is increased to 1. The stress increases in magnitude to about 500 MPa near the bottom of the Ta when the *w/t* ratio is 20. As seen from the plots, the Ta liner-plane stress in the BCB-Cu system increases to potentially damaging values as the *w/t* ratio increases, and this could cause failure of the Ta liner by tensile fracture. In contrast, the Ta liner stress in the SiO_2-Cu system is not significantly affected by the *w/t* ratio of the structure.

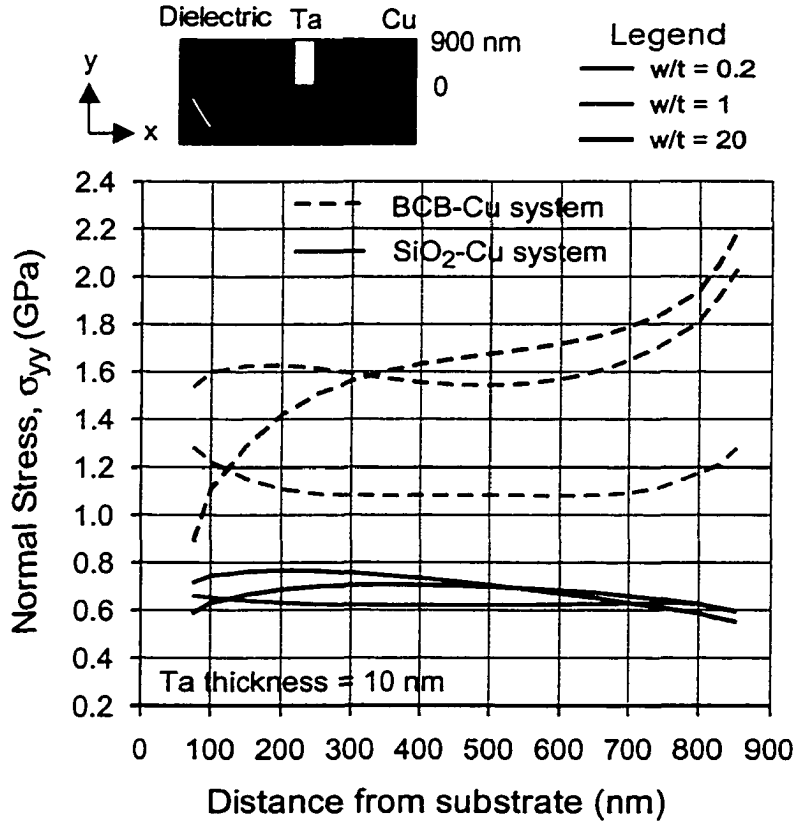


Fig. 4-9 The effect of width-to-thickness (*w/t*) ratio on Ta liner-plane stress in the BCB-Cu and SiO_2-Cu systems with 10 nm thick Ta liners.

The dielectric-Ta interface in both the BCB-Cu and SiO_2-Cu systems is subjected to an in-plane compressive normal stress when the temperature is increased. The plots in **Fig. 4-10** show the effect of the *w/t* ratio on the stress in both interconnection systems.

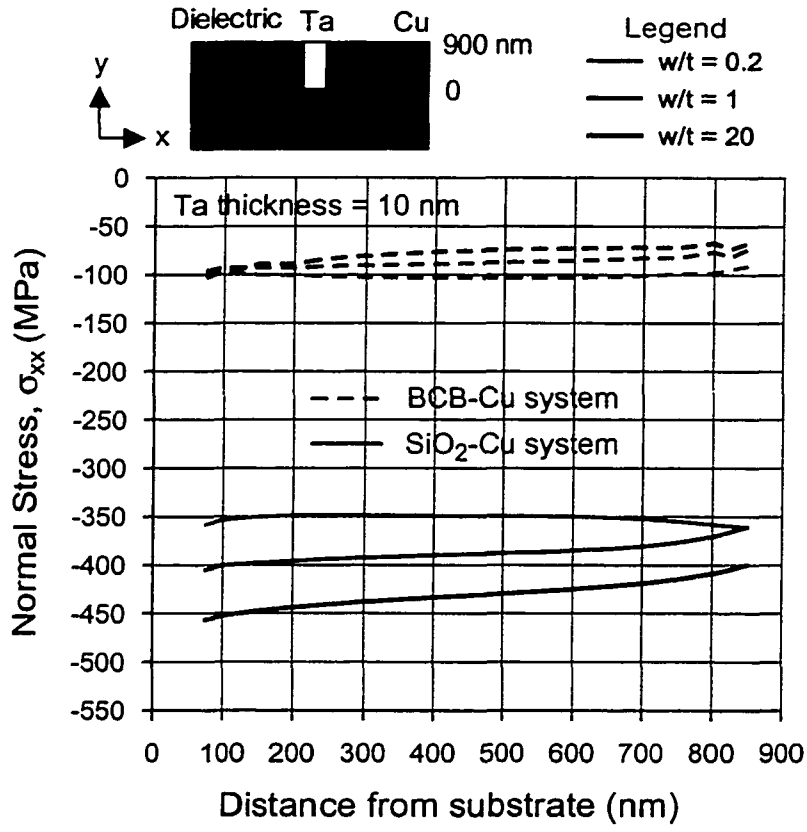


Fig. 4-10 The effect of width-to-thickness (*w/t*) ratio on the in-plane stress normal to dielectric-Ta interface in BCB-Cu and SiO_2-Cu systems with 10 nm thick Ta liners.

As seen from the plots, the stress in the BCB-Cu system is about -100 MPa when the *w/t* ratio is 0.2. The stress decreases by about 30 % (becomes less compressive) when the *w/t* ratio is increased to 1 and by about 50 % when the ratio is increased to 20. The stress near the bottom of the interface is

insignificantly affected. In the SiO_2-Cu system, the in-plane normal stress is about -350 MPa when the *w/t* ratio is 0.2, and it increases by about 20-50 MPa (becomes more compressive) when the *w/t* ratio is increased to 1. When the *w/t* ratio is 20, the compressive stress increases in magnitude by about 50-100 MPa.

The in-plane stress normal to the BCB-Ta interface is relatively small and is insignificantly affected by the *w/t* ratio. The in-plane normal stress in the oxide system is relatively larger and is moderately affected by the *w/t* ratio. A compressive normal stress is not likely to cause failure at the dielectric-Ta interface. However, if the stress on the interface is zero at the peak temperature (400 °C), then the normal stress will be tensile when the structure is cooled to room temperature, and high stresses may result in an interfacial failure.

4-7-2 Effects of the Ta Liner Thickness on Stresses

This section discusses the effect of Ta liner thickness on the dielectric-Ta interfacial stresses and Ta liner stress in the BCB-Cu and SiO_2-Cu systems with *w/t* ratio 1. The plots in **Fig. 4-11** show the effect of Ta liner thickness on the out-of-plane shear stress at the dielectric-Ta interface in both the BCB-Cu and SiO_2-Cu systems, as a result of increasing the Ta liner thickness from 10 nm to 50 nm. As seen from the plots, the Ta liner thickness has only a minor impact on the dielectric-Ta interfacial shear stress in both interconnection systems.

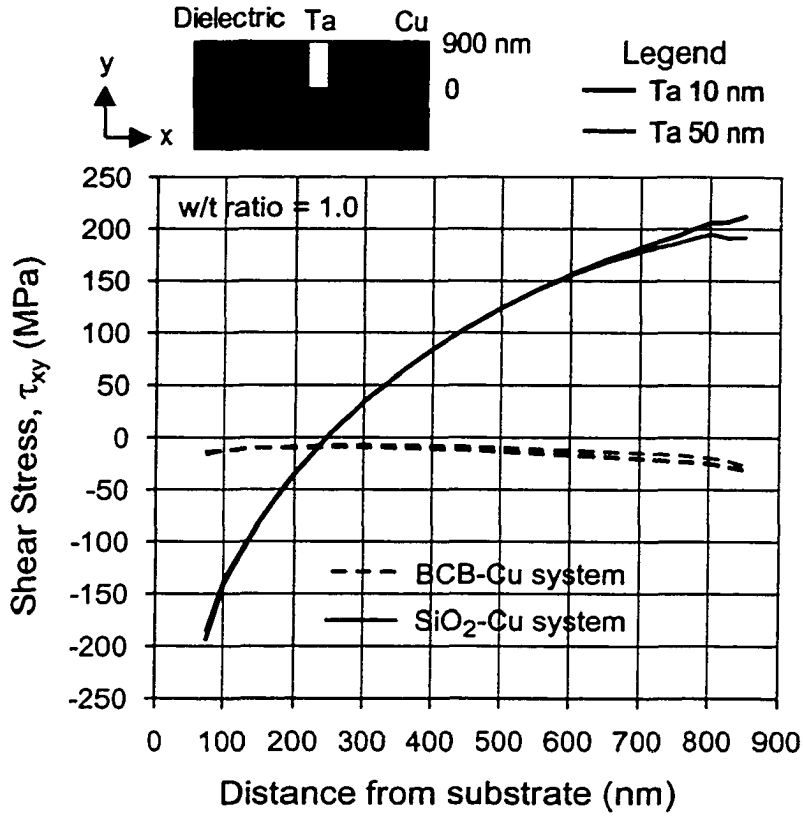


Fig. 4-11 The effect of Ta liner thickness on out-of-plane shear stress at the dielectric-Ta interface in the BCB-Cu and SiO_2-Cu systems when the *w/t* ratio is 1.

Fig. 4-12 shows the effect of varying the Ta liner thickness from 10 nm to 50 nm, on the Ta liner-plane stress in both interconnection systems. It can be seen that the Ta stress in the BCB-Cu structure decreases by 20~25 %, from 1.6 GPa to about 1.3 GPa, when the Ta liner thickness is increased from 10 nm to 50 nm. The Ta stress in the SiO_2-Cu system decreases from 700 MPa to about 600 MPa. Clearly, the Ta liner thickness has minor effects on the Ta liner-plane stress in both interconnection systems. The fact that a five-fold increase in the Ta liner thickness has such a small impact on the Ta stresses indicates that the Ta

thickness is still in the range where stresses in the Ta liner are primarily determined by the CTE mismatch strain between the dielectric and the Ta in both systems.

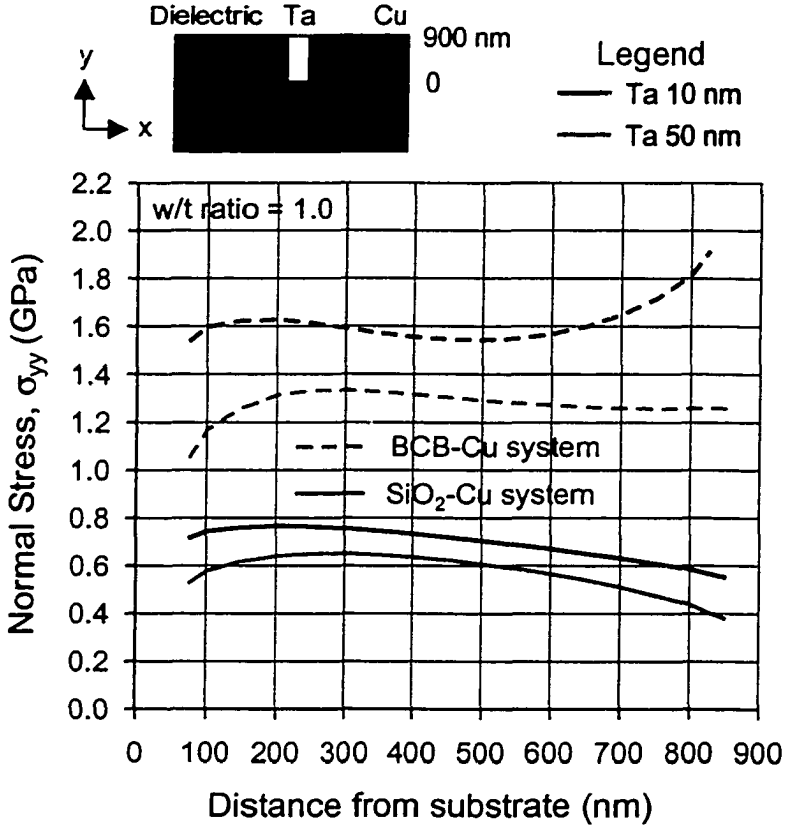


Fig. 4-12 The effect of Ta liner thickness on the Ta liner-plane stress in the BCB-Cu and SiO_2-Cu systems when the *w/t* ratio is 1.

The plots in **Fig. 4-13** demonstrate the effect of varying the Ta liner thickness from 10 nm to 50 nm, on the in-plane stress normal to the dielectric-Ta interface in both interconnection systems. It can be observed that the Ta liner thickness has very small impact of the BCB-Ta normal stress in the BCB-Cu system. The normal stress in the SiO2-Cu system, however, decreases by about

10 %, from –400 MPa to –350 MPa. These are relatively small compressive stresses and are not likely to cause failure of the interface.

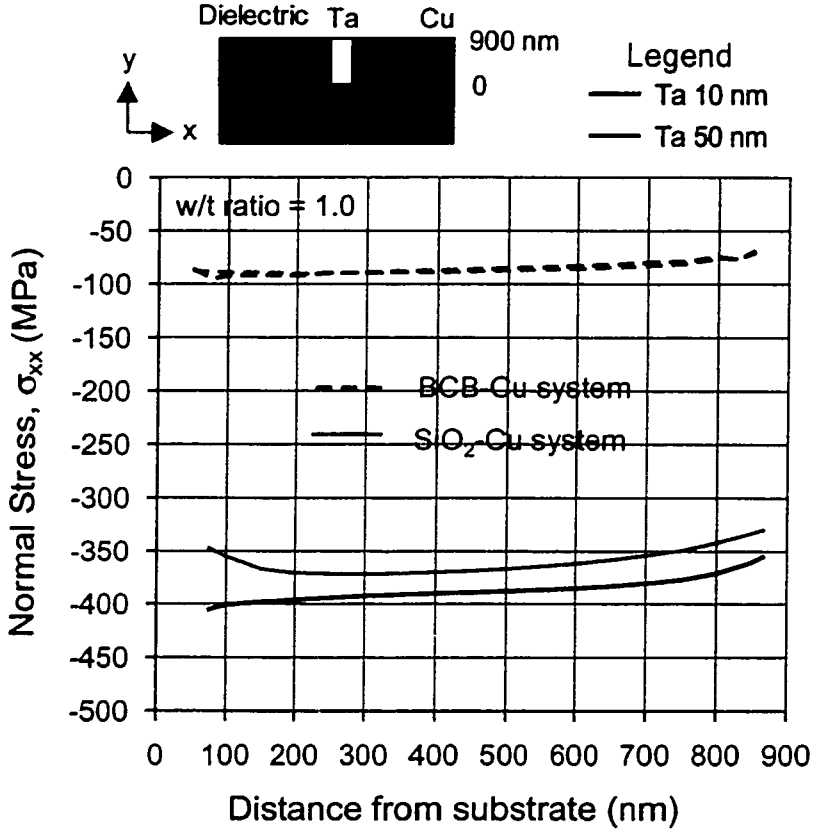


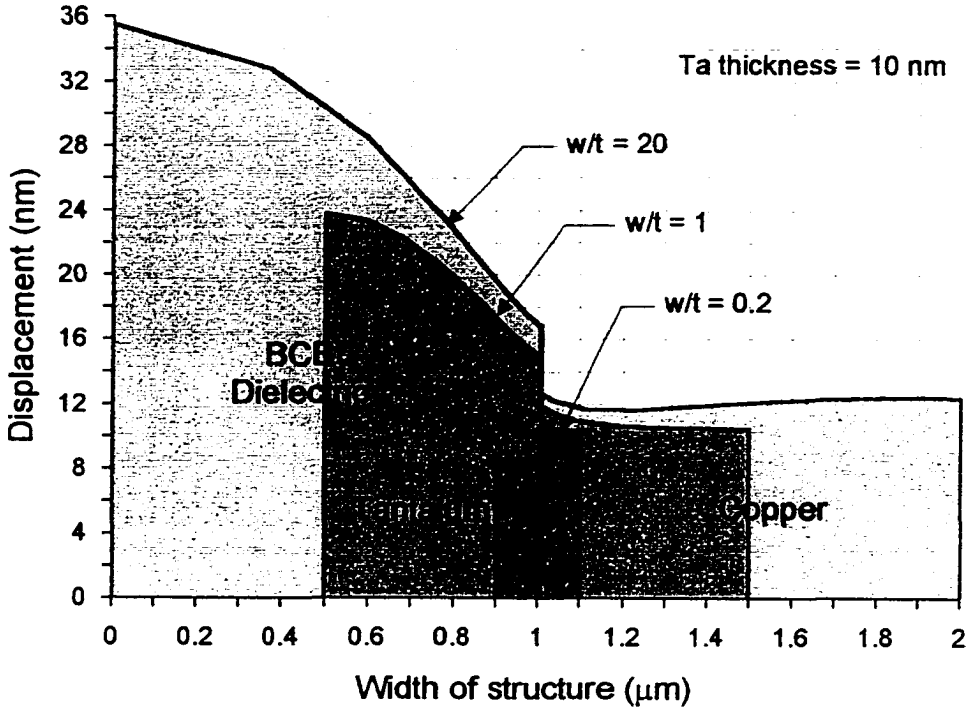
Fig. 4-13 The effect of Ta liner thickness on the in-plane stress normal to the dielectric-Ta interface in the BCB-Cu and SiO_2-Cu systems when the *w/t* ratio is 1.

4-7-3 Effects of Ta Liner Thickness on Direction of Cu-Ta Sliding

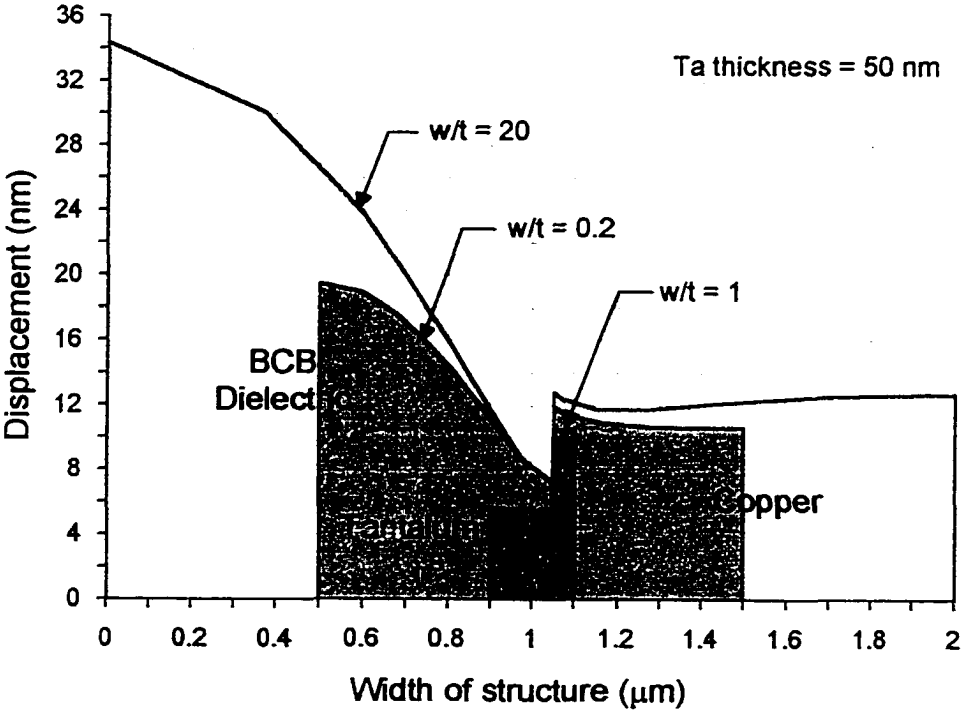
Fig. 4-14 shows plots of the out-of-plane displacement profile across the entire width of the BCB-Cu system, for various *w/t* ratios, after the Cu-Ta sliding. Fig. *4-14(a)* is for 10 nm thick Ta liner while Fig. *4-14(b)* shows the same profile when the Ta liner is 50 nm thick. It can be observed that, with an exception of the *w/t* ratio 0.2, the direction of Cu-Ta interfacial sliding changes from up to down

when the thickness of the Ta liner is increased from 10 nm to 50 nm. The BCB dielectric and the Ta liner slide upwards when the *w/t* ratio is 1 and 20 (*Fig. 4-14(a)*) but both materials slide downwards when the Ta liner is increased by a factor of five (*Fig. 4-14(b)*. It can also be observed that when the *w*/t ratio is 0.2, the downward sliding of the BCB dielectric and the Ta liner increases by approximately 3 nm. The relative elevation of the copper adjacent to the Cu-Ta interface appears to be unaffected by the increase in the Ta liner thickness.

It can also be seen from *Fig. 4-14(a)*, that when the Ta liner is 10 nm thick, the direction of Cu-Ta sliding also changes from up to down as the *w/t* ratio of the structure decreases from 1 to 0.2. The fact that the Ta has such a significant impact on the Cu-Ta sliding behavior is a result of the increasing constraint on the out-of-plane expansion of the BCB dielectric as the Ta liner is increased and as its width decreases (when the Ta liner is 10 nm thick). **Fig. 4-15** shows the plots of out-of-plane displacement profile across the width of the SiO_2-Cu structures, for various *w/t* ratios. *Fig. 4-15(a)* shows the profiles for 10 nm thick Ta liner while *Fig. 4-15(b)* shows the plots for 50 nm thick Ta liner. It can be seen that the Ta liner thickness has a negligible effect on the direction of the Cu-Ta sliding because the oxide dielectric, Ta liner, and copper have approximately the same order of magnitude of elastic constants, *E*. For all the *w/t* ratios, the dielectric and Ta liner slide down relative to the interface. The relative elevation of copper adjacent to the Cu-Ta interface is also unaffected by the Ta liner thickness.

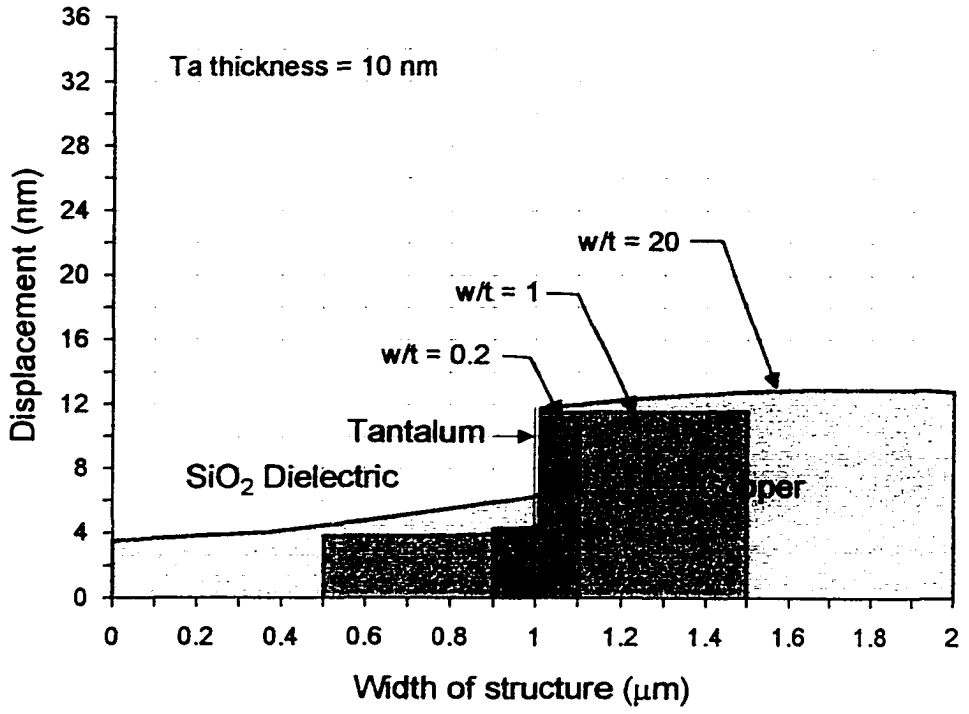


(a)

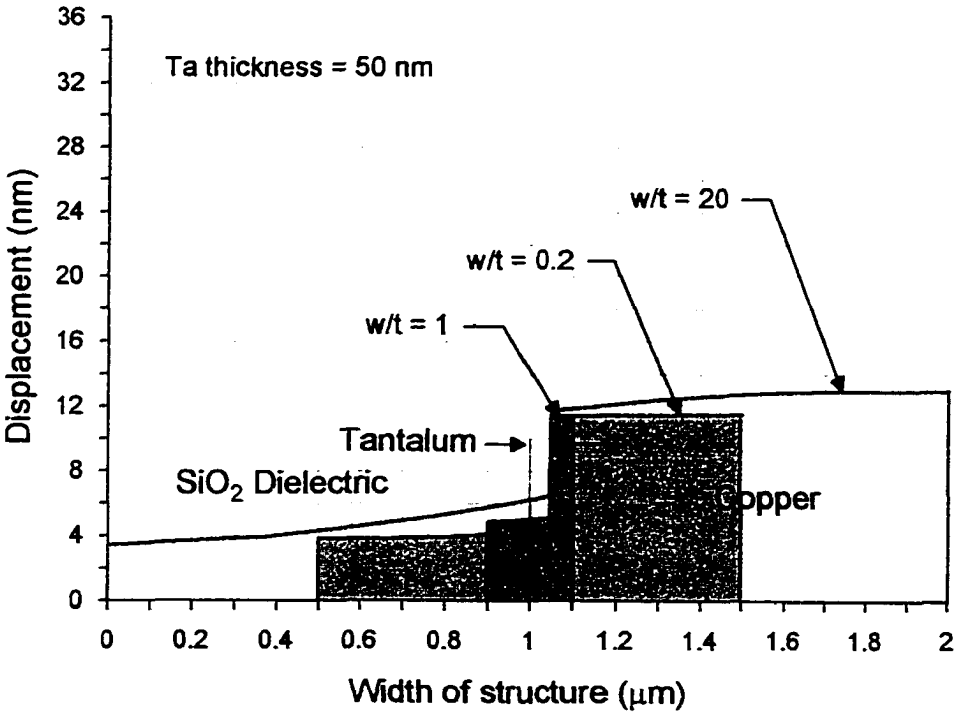


(b)

Fig. 4-14 The effect Ta liner thickness on direction of Cu-Ta sliding in the BCB-Cu system, for various *w/t* ratios. (a) Ta liner is 10 nm thick, and (b) Ta liner is 50 nm thick.



(a)



(b)

Fig. 4-15 The effect Ta liner thickness on direction of Cu-Ta sliding in the SiO_2-Cu system for different *w/t* ratios. (a) Ta liner is 10 nm thick, and (b) Ta liner is 50 nm thick.

4-7-4 Relaxation of Shear Stress at Cu-Ta Interface

The Cu-Ta sliding causes the out-of-plane shear stress at the interface to relax to a negligibly small value. **Fig. 4-16** shows variation of the shear stress with time, at a representative node on the Cu-Ta interface in the BCB-Cu system. The shear stress data fits nicely to an exponential function given by

$$\sigma_{xy} = 137.12 \cdot \exp\left(-\frac{t}{\tau}\right)$$

where τ is a *stress relaxation time constant*. For this particular structure, τ is approximately 0.07 seconds. It can be seen that the shear stress is relaxed to a negligible value after about 5τ seconds.

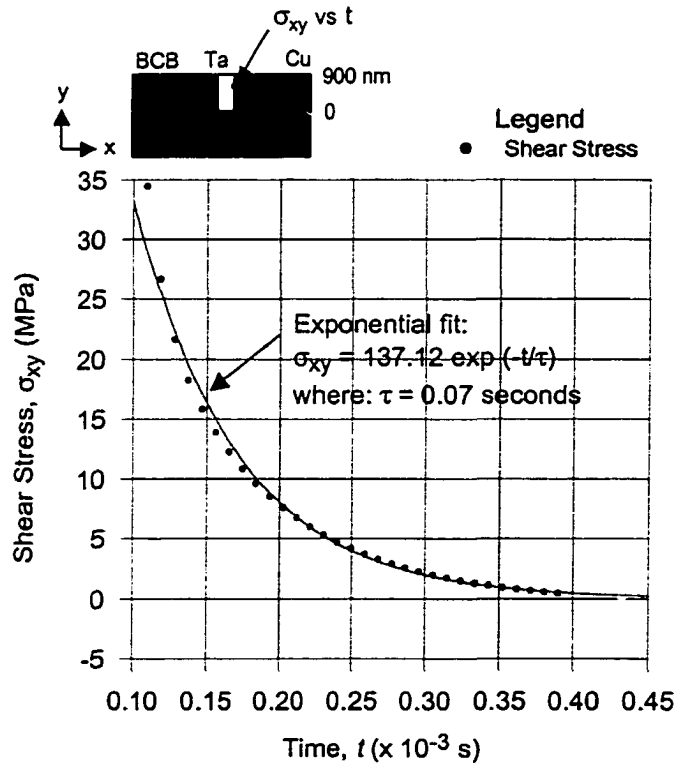


Fig. 4-16 Shear stress at Cu-Ta interface relaxed in exponential decay with time due to the sliding.

Fig. 4-17 shows the effect of temperature on the stress relaxation time constant τ, for both BCB-Cu and SiO_2-Cu interconnection systems, obtained by extrapolation of the finite element results. It can be seen that, for a given temperature, *w/t* ratio and Ta thickness, the rate of shear stress relaxation in the SiO_2-Cu system (which is proportional to $1/\tau$) is about 4 times faster than in the BCB-Cu system. At 400 °C, the shear stress in both systems are relaxed in fractions of a second, while at 25 °C, the shear stress in the SiO_2 system would completely relax in days whereas the shear stress in the BCB-Cu system would require a much longer time to be relaxed completely.

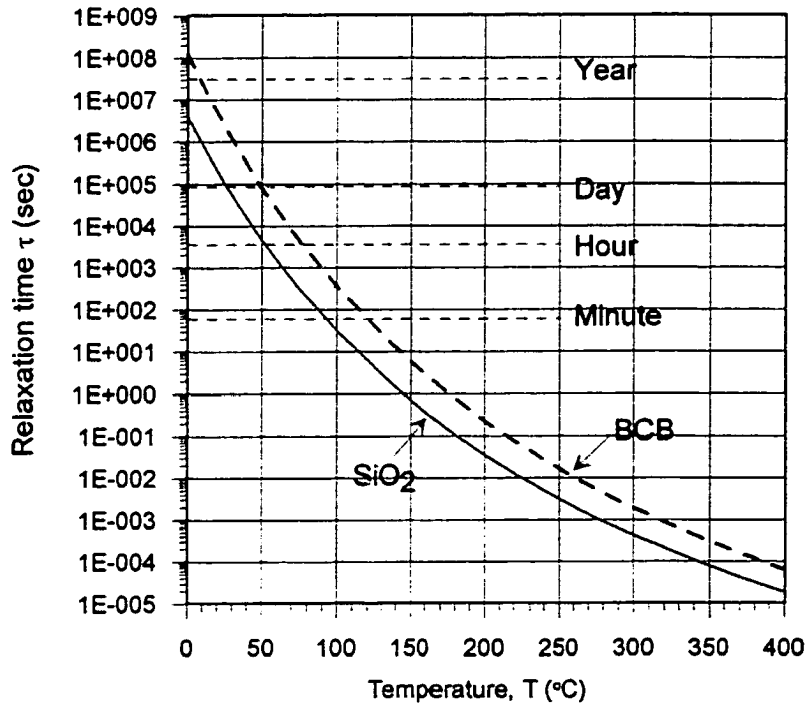


Fig. 4-17 Variation of stress relaxation time constant τ with temperature for both BCB-Cu and SiO_2-Cu systems. For a given temperature, *w/t* ratio and Ta liner thickness, the rate of stress relaxation in the SiO_2-Cu system is about 4 times faster than in the BCB-Cu system.

4-7-5 Effects of Cu-Ta Sliding on Out-of-Plane Shear Stress

The effects of the Cu-Ta sliding on the stresses at the dielectric-Ta interface in the BCB-Cu and SiO_2-Cu systems were evaluated by comparing the state of the stresses *before* and *after* the sliding. The evaluation was made only in the structures having a 10 nm thick Ta liner, but for various *w/t* ratios.

Fig. 4-18 shows the effect of the Cu-Ta sliding on the out-of-plane shear stress at the BCB-Ta interface in the BCB-Cu interconnection system.

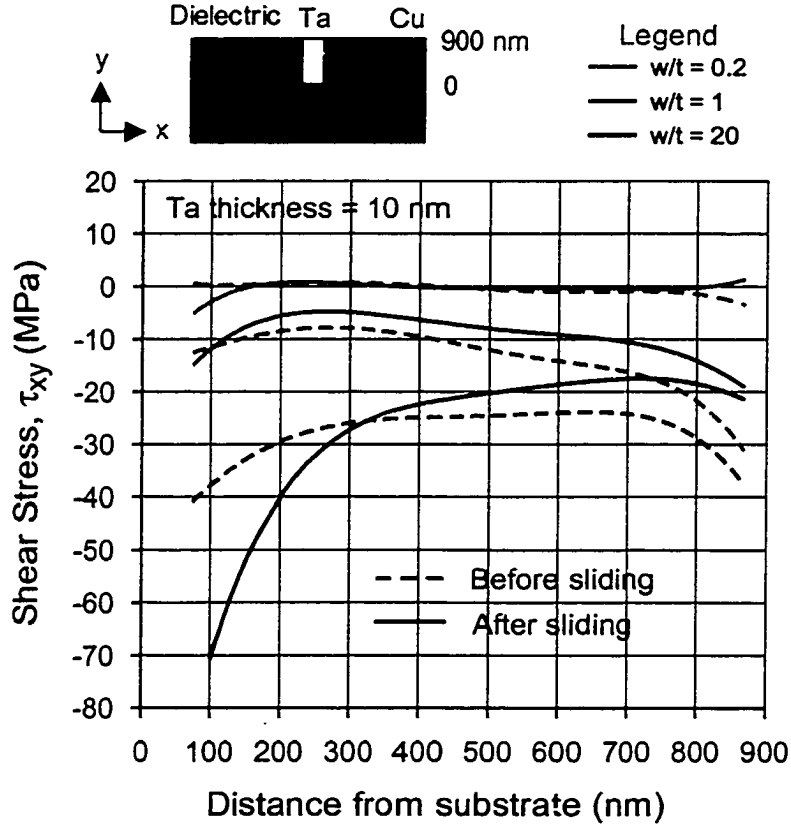


Fig. 4-18 The effects of Cu-Ta sliding on out-of-plane shear stress at BCB-Ta interface in the BCB-Cu system, for various *w/t* ratios, when the Ta liner is 10 nm thick.

It can be seen that when the *w/t* ratio is 0.2, the Cu-Ta sliding has very little impact on the BCB-Ta shear stress. However, when the *w/t* ratio is increased to 1, the shear stress is relaxed by about 20-40 %. The shear stress near the top is relaxed by about 30 % but it increases by nearly 75 % near the bottom of the interface, when the *w/t* ratio is 20. As the upper part of the interface experience the sliding, the strain due to the CTE mismatch between BCB and the Ta liner has to be supported by the bottom part, resulting in increase in the shear stress near the bottom. However, the dielectric-Ta shear stress in BCB-Cu system is relatively small for all *w/t* ratios, as seen from the figure. Thus, the Cu-Ta interfacial sliding is not expected to have any serious impact on the shear strength of the BCB-Ta interface.

Fig. 4-19 shows the effect of the Cu-Ta sliding on the SiO_2-Ta shear stress in the SiO_2-Cu interconnection system. As seen from the plots, for all *w/t* ratios, the shear stress at the SiO_2-Ta interface is completely relaxed to a relatively small value as a result of the sliding. This trend is expected since the oxide dielectric and the Ta liner slide downward relative to the Cu-Ta interface due to the interfacial sliding (see **Fig. 4-15**). Since the out-of-plane interfacial shear stress is one of the major causes of interfacial failure in metal-oxide dielectric interconnect structures, the Cu-Ta interfacial sliding could be an important shear stress relaxation mechanism for this system.

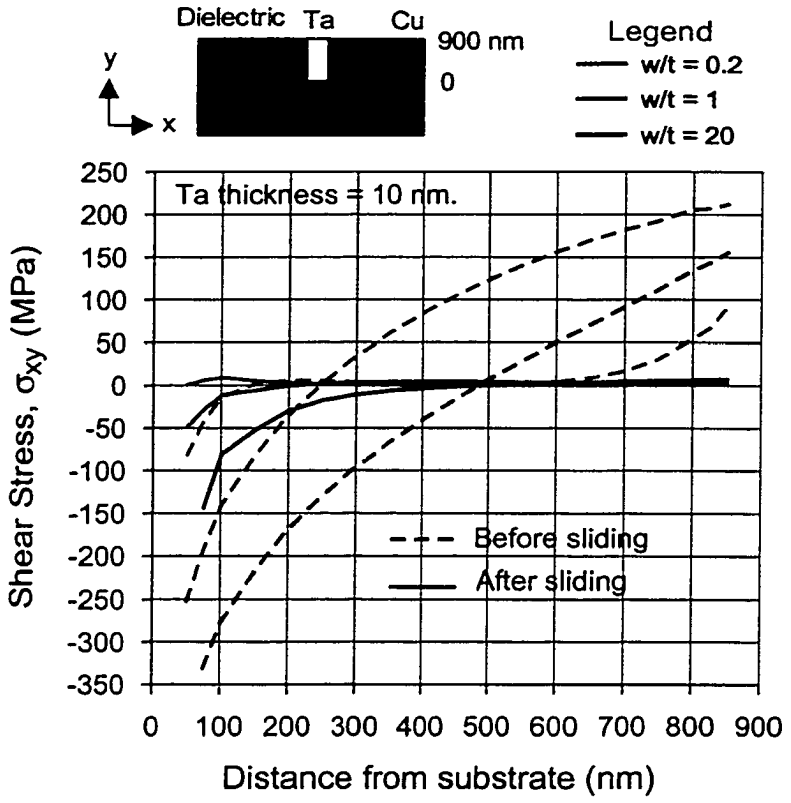


Fig. 4-19 The effects of Cu-Ta sliding on the shear stress at SiO_2-Ta interface in the SiO_2-Cu system, for various *w/t* ratios, when the Ta liner is 10 nm thick.

4-7-6 Effects of Cu-Ta Sliding on Ta Liner-Plane Stress

The Ta liner is subjected to a tensile stress normal to the plane of the film, as the temperature is raised from 20 °C to 400 °C. **Fig. 4-20** shows the effects of Cu-Ta sliding on the liner stress in the tantalum in the BCB-Cu structure, for various *w/t* ratios. It can be seen that the Ta stress is relaxed by about 200 MPa when the *w/t* ratio is 0.2. However, when the ratio is increased to 1, the Ta stress increases in magnitude by about 800 MPa, which is a very significant stress increment. These are expected because when the *w/t* ratio is 0.2, the dielectric and

the Ta liner slide downward due to the Cu-Ta sliding but the materials slide upward relative to the interface when the *w/t* ratio is 1 (see **Fig. 4-14**). The Ta liner-plane stress increases by about 1.5 GPa (on average) when the *w/t* ratio is increased to 20. The greatest stress increment occurs near the bottom of the Ta where the stress increases to about 4 GPa. This is a huge stress increment and it could cause the Ta liner to fail by tensile fracture, thus severely impacting the mechanical integrity and reliability of the entire structure.

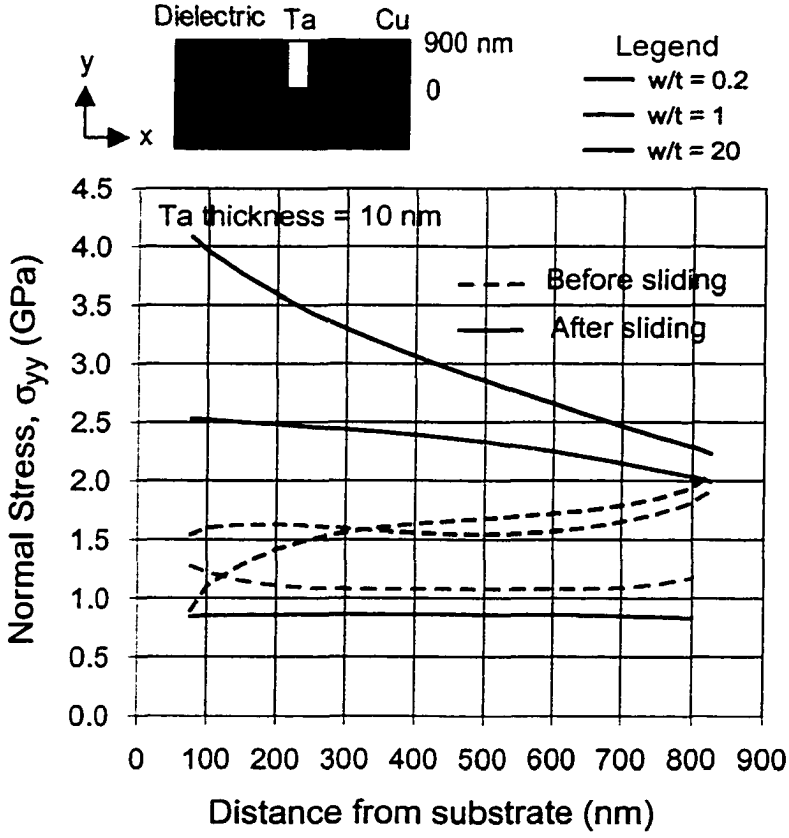


Fig. 4-20 The effects of Cu-Ta sliding on the Ta liner-plane stress in BCB-Cu system, for various *w/t* ratios, when the Ta liner is 10 nm thick.

The above observations suggest that prevention of sliding at the Cu-Ta interface in the BCB-Cu system having large *w/t* ratios would lessen the probability of tensile failure of the Ta liner. Fabrication of the *dual-damascene* BCB-Cu interconnect structure for instance, could accomplish this goal.

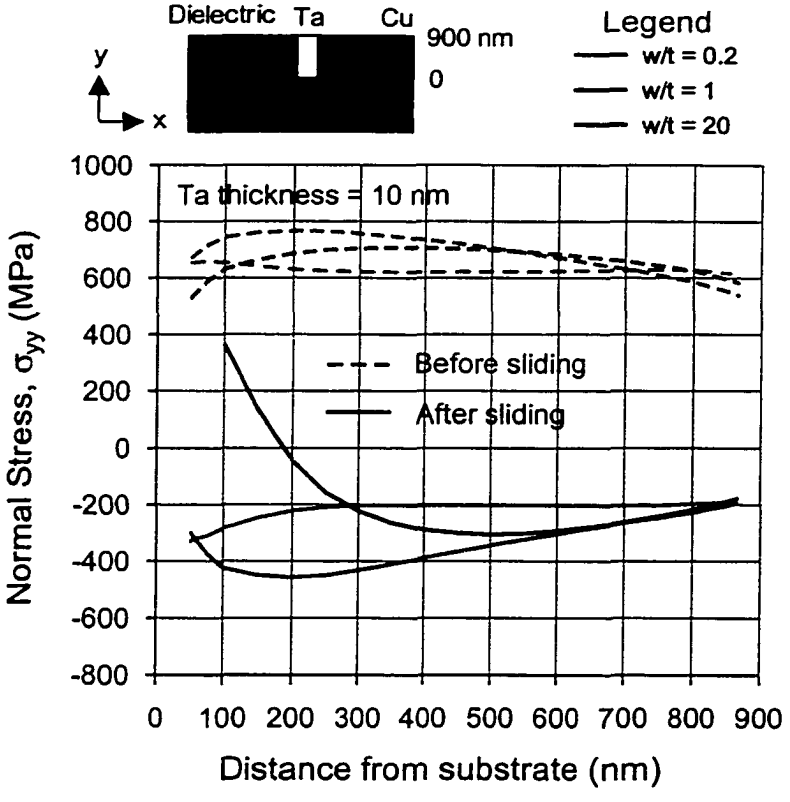


Fig. 4-21 The effects of Cu-Ta sliding on the Ta liner-plane stress in SiO_2-Cu system, for various *w/t* ratios, when the Ta liner is 10 nm thick.

Fig. 4-21 shows the effect of Cu-Ta interfacial sliding on the Ta liner-plane stress in the SiO_2-Cu system, for various *w/t* ratios. It can be seen that for a given *w/t* ratio, the sliding causes the Ta stress to change sign, from about 700 MPa to about –300 MPa. However, the stress near the bottom of the Ta remains positive

(at about 400 MPa) when the *w/t* ratio is 20. This may be attributed to the excessive bending of the Ta liner due to an increase in the in-plane stress normal to the SiO_2-Ta interface, which prevented the Cu-Ta sliding near the bottom to fully-relaxed the Ta stress. In general, Cu-Ta interfacial sliding in SiO_2-Cu interconnection system has a positive impact on the Ta liner plane stress.

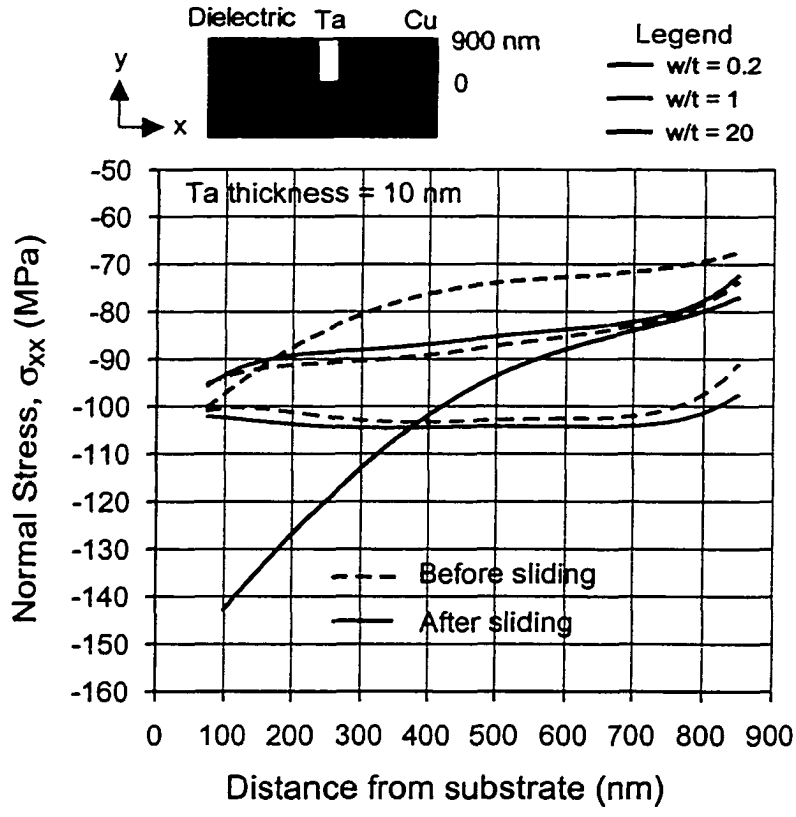


Fig. 4-22 The effects of Cu-Ta sliding on the in-plane stress normal to the BCB-Ta interface, for various *w/t* ratios, when the Ta liner is 10 nm thick.

4-7-7 Effects of Cu-Ta Sliding on In-plane Normal Stress

Fig. 4-22 shows the effect of Cu-Ta sliding on the in-plane stress normal to the dielectric-Ta interface in the BCB-Cu system, for various *w/t* ratios, when the

Ta liner is 10 nm thick. It can be seen from the figure that the Cu-Ta sliding has a negligibly small effect on the BCB-Ta normal stress when the *w/t* ratio is small, but when the ratio is 20, the compressive normal stress increases in magnitude by about 10-40 MPa. However, these are relatively small stresses and therefore are not expected to have any significant impact on the interfacial strength in the BCB-Cu interconnection system.

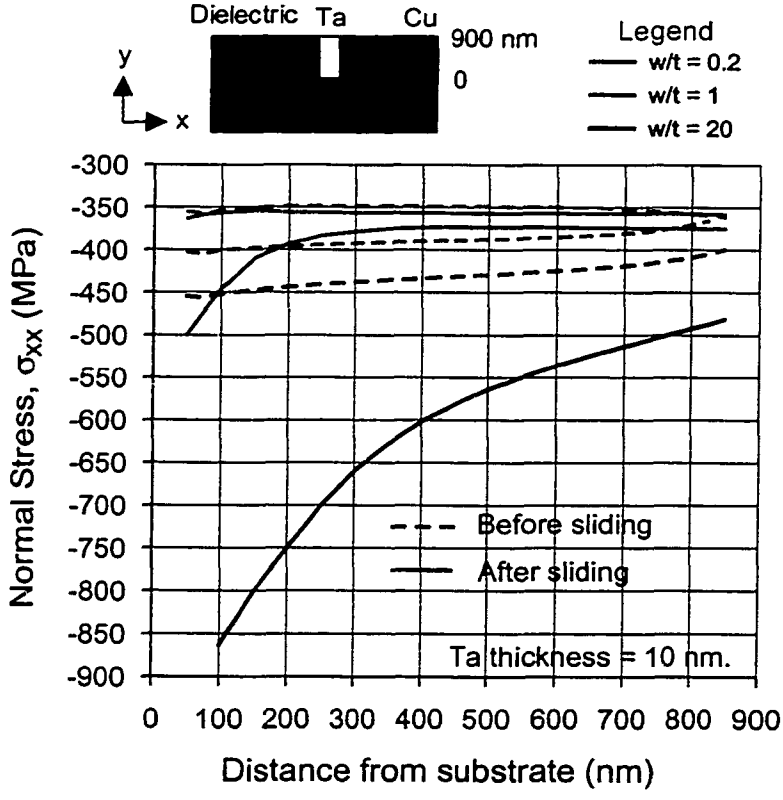


Fig. 4-23 The effects of Cu-Ta sliding on the in-plane stress normal to the SiO_2-Ta interface, for various *w/t* ratios, when the Ta liner is 10 nm thick.

The effect of Cu-Ta sliding on the in-plane normal stress at the SiO_2-Ta interface in the SiO_2-Cu system is shown in **Fig. 4-23**. As in the BCB-Cu system,

the Cu-Ta sliding also has a negligibly small impact on the stress when the *w/t* ratio of the structure is small. However, when the *w/t* ratio is 20, the sliding causes the SiO_2-Ta in-plane normal stress to increase in magnitude by about 100-400 MPa, in which the largest stress increment occurred at the bottom half of the interface. Although this is a significant stress increment, compressive normal stress is less likely to have an adverse impact on the interfacial strength.

4-8 Effects of Copper Grain Boundary Sliding

In this study, a finite element method is also used to simulate the sliding at copper grain boundary in the BCB-Cu system having *w/t* ratio 20 and Ta liner thickness 10 nm. The goal is to evaluate its impact on the Cu-Ta sliding and relaxation of interfacial shear stress. The Cu-Cu sliding effect was produced by incorporating a 1 nm thick sliding element in the copper, at 500 nm away from the Cu-Ta interface. The Cu-Cu sliding element has creep properties identical to that for the Cu-Ta sliding element (see **Table (4-3)**) except that the sliding rate was proposed to be twice as fast. During the finite element simulation, temperature was held constant at 400 °C immediately after the heating, to allow both the Cu-Ta and Cu-Cu sliding effects to occur simultaneously.

4-8-1 Effects of Cu Grain Boundary Sliding on Cu-Ta Interfacial Sliding

Fig. 4-24 shows a profile plot of out-of-plane displacement across the entire width of the BCB-Cu structure. The dashed line is the displacement profile

when only Cu-Ta sliding occurs while the solid line is that when both Cu-Ta and Cu grain boundary sliding occur simultaneously.

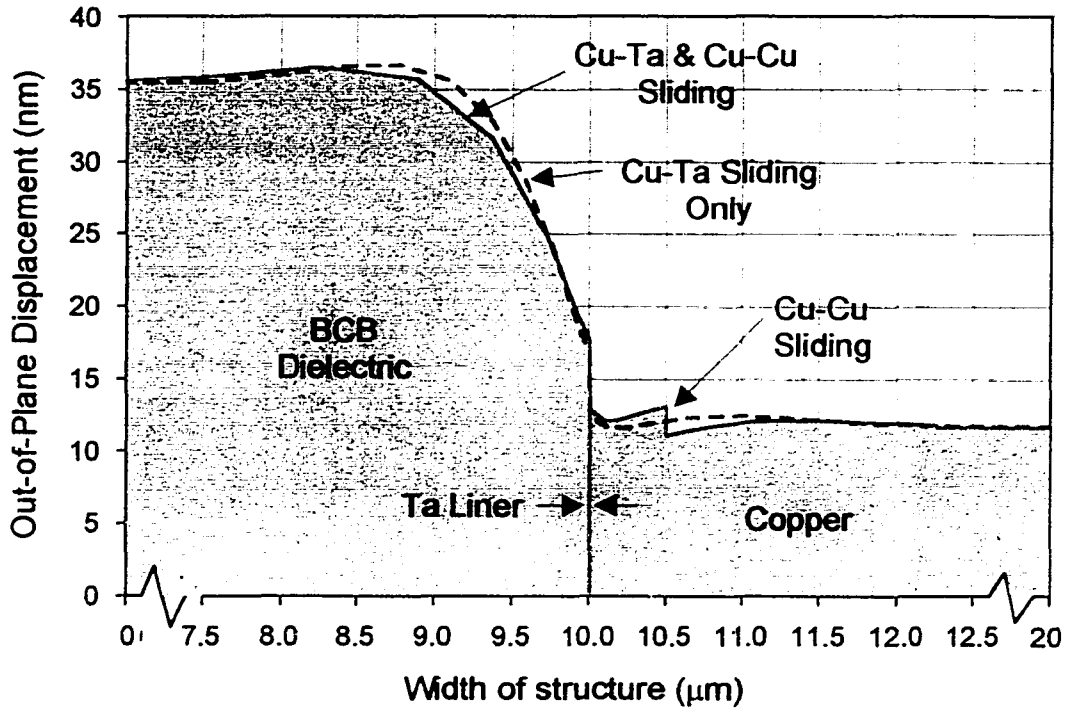


Fig. 4-24 Plots of *y*-displacement profile at the top surface of the BCB-Cu structure showing the effect of Cu grain boundary sliding on the interfacial sliding at the Cu-Ta interface.

It can be observed from the figure that the Cu grain boundary sliding produces a 2-3 nm relative step height at the Cu grain boundary, on the surface. The BCB dielectric is depressed by approximately 2-3 nm at about 1 μm away from the Cu-Ta interface. The displacement profile of both the BCB dielectric and the copper further away from the Cu-Ta interface appear to be unaffected by the Cu grain boundary sliding. The interfacial sliding at the Cu-Ta interface does not appear to be significantly affected by the Cu grain boundary sliding.

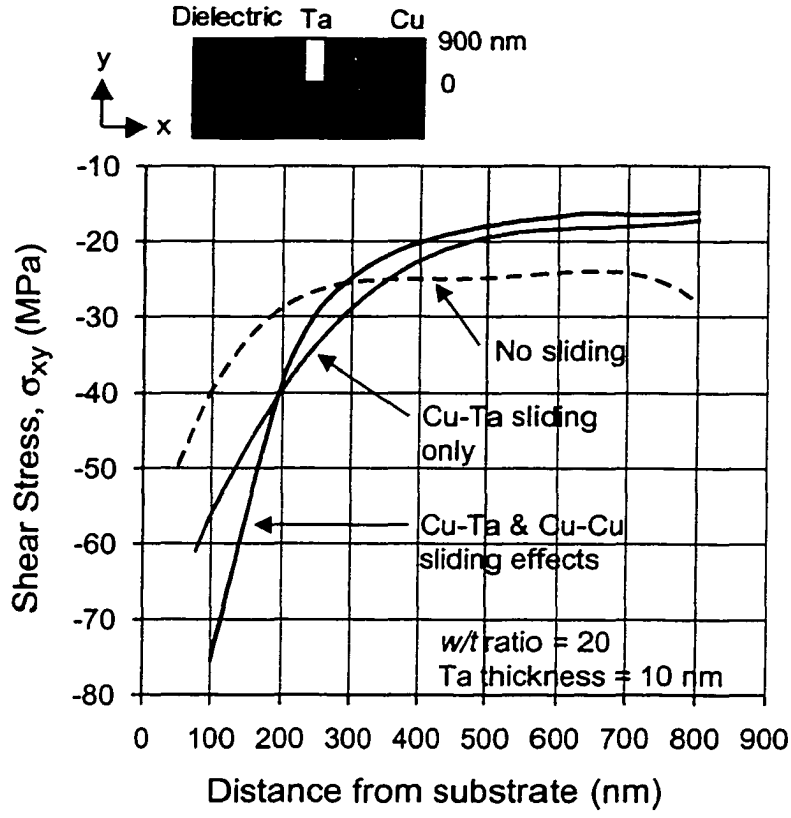


Fig. 4-25 The effects of Cu grain boundary sliding on the relaxation out-of-plane shear stress at the BCB-Ta interface. The *w/t* ratio is 20 and Ta liner is 10 nm thick.

4-8-2 Effects of Cu Grain Boundary Sliding on BCB-Ta Shear Stress

The plot in Fig. 4-25 shows the effect of the Cu grain boundary sliding on the relaxation of the shear stress at the BCB-Ta interface. As seen from the figure, the out-of-plane shear stress along the upper half of the BCB-Ta interface decreases further by about 10-20 % (become less negative) when the Cu grain boundary sliding occurs along with the Cu-Ta sliding. The shear stress along the bottom half of the interface increases by about 20-30% (becomes more negative) due to the presence of the Cu grain boundary sliding. Note that, as the Cu-Ta

interfacial sliding is allowed to occur at the Cu-Ta interface, the lower part (where the sliding is limited by the Si substrate) has to work "harder" to support the CTE mismatch strain between the BCB and the Ta liner and thus to maintain the structural integrity at the interface. This results in increasing negative shear stress at the bottom part of the BCB-Ta interface. The stress increases even further when the Cu-Cu sliding is also allowed to occur in the copper. However, the shear stress at this interface is small in magnitude. Although the shear stress increases slightly due to the Cu grain boundary sliding, it is not likely to have a significant impact on the shear strength of the interface.

4-9 Effects of Assuming Zero Stresses at 20°C

The finite element simulations of the Cu-Ta sliding in both BCB-Cu and SiO_2-Cu structures were performed with the assumption that the stresses in both structures are zero at 20 °C. This may not be the case in the real structures since each material component is deposited at different elevated temperatures. The CTE mismatch between the material components would result in residual stresses in the structures, upon cooling to room temperature.

The BCB and other polymer dielectrics are usually spin-coated and cured at elevated temperatures of 350°C to 400°C. Upon cooling to room temperature, the film is subjected to a biaxial tensile stress due to the in-plane CTE mismatch with the thick Si substrate. However, circuit patterns definition on the film by a

combination of photolithography and reactive ion etching (RIE) processes will relieve much of the stresses, especially in the structures with narrow dielectrics. Most oxide dielectrics are deposited either by chemical vapor deposition (CVD) technique or by spin coating, also at elevated temperatures. The in-plane CTE of the silicon dioxide (SiO_2) dielectric and the Si substrate are nearly the same, so the in-plane stresses in the oxide will be small regardless of the dielectric deposition temperatures. The assumption that the stresses in the BCB and SiO_2 dielectric are zero at room temperature (20 °C) is therefore reasonable, based on these situations.

The Ta liner is usually deposited by physical vapor deposition (PVD) or by plasma enhanced chemical vapor deposition (PECVD) at elevated temperatures. The out-of-plane CTE of most polymer films are at least an order of magnitude greater than the Ta. When the polymer-Cu structures are cooled to room temperature, the Ta liner will likely to be subjected to compressive stresses normal to the plane of the film. This effect is desirable, as it will help reduce the magnitude of potentially damaging tensile stress in the Ta liner, when the structures are heated to peak processing temperatures during the fabrication of multi-level interconnection structures. Therefore, one can expect that high Ta deposition temperatures would enhance Ta liner reliability in Cu-polymer dielectric systems.

In contrast, the Ta liner in the oxide-Cu systems would be subjected to tensile stresses normal to the film's plane upon cooling to room temperature, because the out-of-plane CTE of the Ta is greater than the SiO_2 dielectric. For a given *w/t* ratio and 10 nm thick Ta liner, the stresses would be approximately equal and opposite to the Ta liner-plane stresses after the Cu-Ta sliding (see **Fig. 4-21**). These tensile stresses will increase as the structure is brought to elevated temperatures because the out-of-plane CTE of the copper is greater than the Ta, but the Cu-Ta sliding will decrease the magnitude of the stresses. The as-deposited Ta liner-plane tensile stresses in the oxide-Cu systems are therefore undesirable. However, the stresses are reasonably low (less than 1 GPa), so the Ta deposition temperature should not have negative effects on the Ta liner reliability.

The behavior of the copper is the most complex. Copper is known to exhibit time-dependent deformation (diffusional flow creep) at the elevated temperatures that will relax the stresses. The deformation map of a 3 μm x 4 μm copper via shown in **Fig. 4-4(a)** indicates that the deformation of Cu is non-uniform. Electrodeposited copper has been observed to undergo extensive *recrystallization* at the room temperature [29], [30] which will relieve most of the stresses. Therefore, the assumption that the stresses in the Cu are zero at room temperature, in both the BCB-Cu and the SiO_2-Cu interconnect structures, is also reasonable.

4-10 Summary of the Effects of Cu-Ta Sliding

A finite element method was used to model the Cu-Ta interfacial sliding and Cu grain boundary sliding in a 1 μm thick single level damascene copper interconnect structures, at 400 °C. It was shown that the out-of-plane shear stress at the Cu-Ta interface in both the BCB-Cu and the SiO_2-Cu systems are relaxed in exponential decay with time, and for a given *w/t* ratio and Ta liner thickness, the rate of stress relaxation in the SiO_2 system is nearly 4 times faster than in the BCB system. Except for *w/t* ratio of 0.2, the direction of the Cu-Ta sliding in BCB-Cu system changes from up to down when the Ta liner thickness increases from 10 nm to 50 nm. When the Ta liner is 10 nm thick, the direction of the Cu-Ta sliding also changes from up to down when the *w/t* ratio decreases from 1 to 0.2. In contrast, the direction of the Cu-Ta sliding in the SiO_2-Cu system was unaffected by either the Ta liner thickness or the *w/t* ratio.

The Cu-Ta sliding has a negligible effect on interfacial shear stress in the BCB-Cu system. In contrast, the shear stresses in the SiO_2-Cu system are completely relaxed to negligible values, for all *w/t* ratios. The Cu-Ta sliding has a potentially damaging effect that could cause tensile fracture of the Ta liner in the BCB-Cu system, especially when the *w/t* ratio is large. The sliding has a positive effect on the Ta liner in the SiO_2-Cu system in which the Ta liner stress changes from tensile to compressive, for all *w/t* ratios. The sliding has only a minor impact on the in-plane normal stress in both interconnection systems.

Cu grain boundary sliding has a negligibly small impact on the interfacial sliding at the Cu-Ta interface and the relaxation of interfacial shear stress in the BCB-Cu system having *w/t* ratio *20* and Ta liner thickness of *10* nm.

Chapter 5

FINITE ELEMENT MODELING OF *NABARRO-HERRING* CREEP DEFORMATION

5-1 Creep Deformation

In addition to elastic and plastic deformation, materials deform by mechanisms that result in markedly time-dependent behavior, called *creep*. Under a constant applied stress, the strain varies with time as shown in **Fig 5-1.** There is an initial elastic deformation, and following this, the strain slowly increases as long as the stress is maintained. If the stress is removed, the elastic strain ε_e is quickly recovered, and a portion of the creep strain may be recovered slowly with time while the rest remains as permanent deformation.

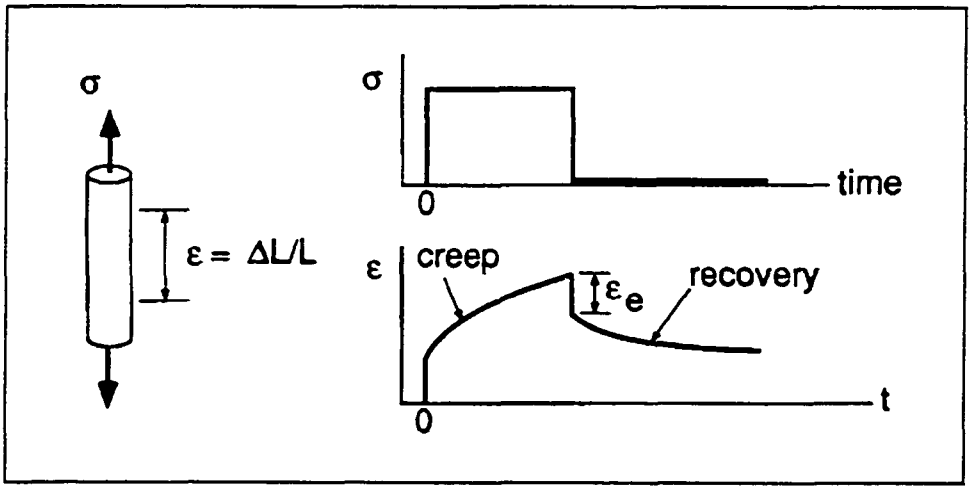


Fig. 5-1 Accumulation of creep strain with time under constant stress, and partial recovery after removal of the stress.

In crystalline materials (metals and ceramics), one important mechanism of creep is diffusional flow of vacancies. Vacancies are more easily accommodated near grain boundaries under compressive strain but less easily accommodated near those under tensile strain. Thus, they tend to move in a slow time-dependent manner (or to diffuse) from some regions within a grain to others, as illustrated in **Fig. 5-2**. As indicated, movement of vacancy in one direction is equivalent to movement of an atom in the opposite direction. The overall effect of this process is a change in shape of the grain, contributing to microscopic creep strain.

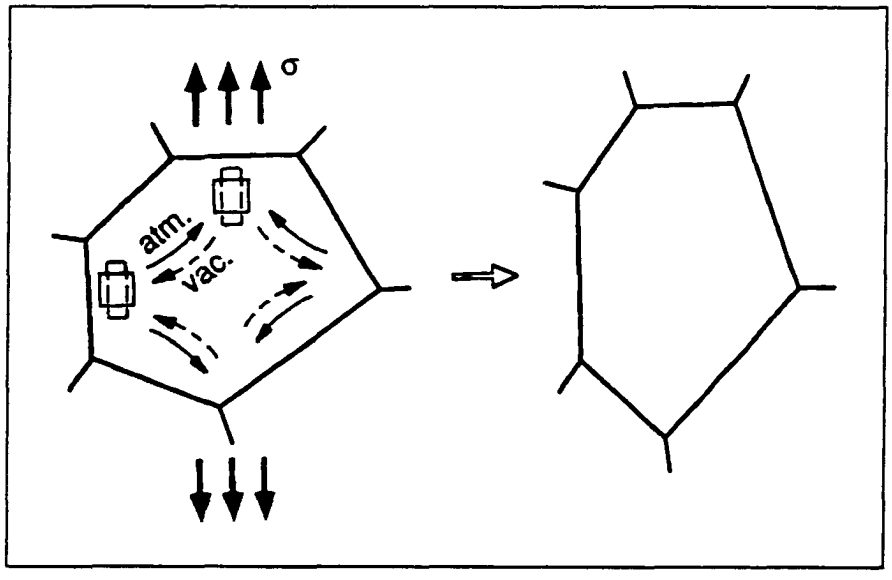


Fig. 5-2 Mechanism of creep by diffusion of vacancies within a crystal grain.

Some other creep mechanisms that operate in crystalline materials include special dislocation motions that can circumvent obstacles in a time-dependent manner. There may also be sliding of grain boundaries and the formation of

cavities along grain boundaries. Creep behavior in crystalline materials is strongly temperature dependent, typically becoming an important engineering consideration around 0.3 - 0.6 T_m, where T_m is the absolute melting temperature of the material.

5-2 Diffusion of Vacancies

A vacancy is a point defect in crystalline material, caused by an atom simply not appearing at an atom site, as illustrated in **Fig. 5-3(a)**. Diffusion by the vacancy flow mechanism is illustrated in **Fig. 5-3(b).** For atom 1 shown in the figure to move into the adjacent vacant site, it must squeeze past atoms 2 and 3. The *activation energy for vacancy motion, Q_m,* is the energy required to move these atoms apart. If the solid is composed of a single element, such as pure copper, the movement of the atom is called *self-diffusion* because the moving atom and the solid are of the same chemical element.

Diffusion by vacancy flow mechanism in solid materials is described mathematically by two differential equations, known as *Fick's* laws. The *Fick's* first law is expressed as:

$$J_v = -D_v \cdot \frac{dC_v}{dx} \qquad (5\text{-}1)$$

where J_v is the *net* mass flow-rate or *flux* of vacancy and D_v is the *diffusivity* or the *vacancy diffusion coefficient.* Quantity (dC_v/dx) is called *vacancy concentration*

gradient in the *x*-direction. The *minus* sign indicates that vacancies flow from a high concentration region towards the lower concentration region.

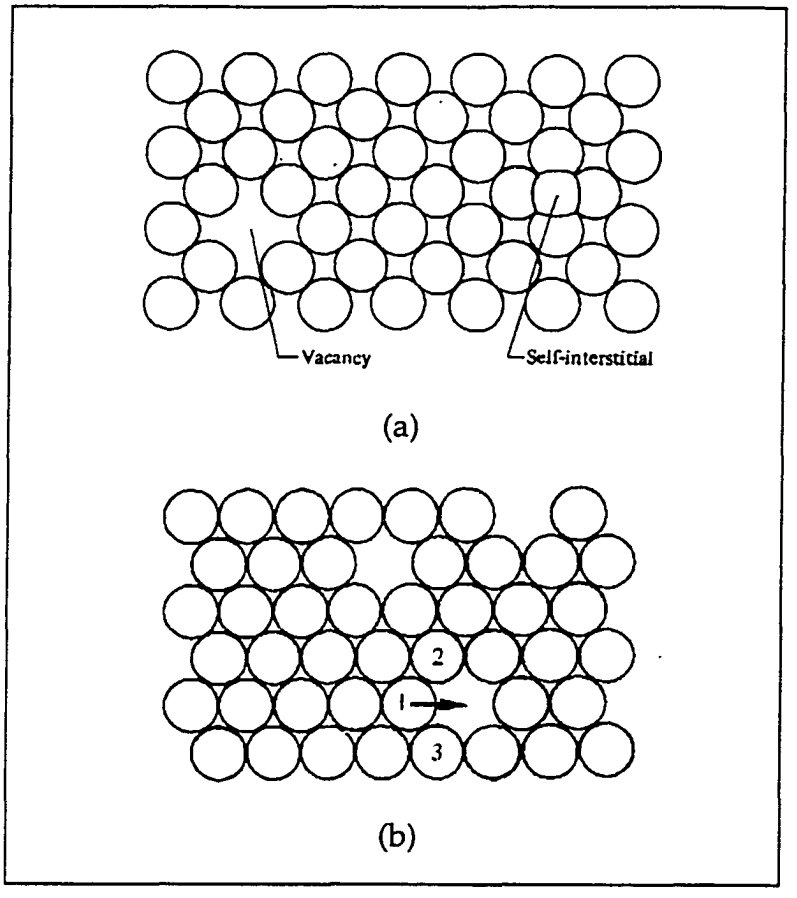


Fig. 5-3 (a) A plane of atoms in a crystal showing a vacancy and a self-interstitial, which are point defects. (b) Atomic diffusion by vacancy flow mechanism in a pure solid material.

Fick's first law allows one to compute an instantaneous mass flow rate or *flux* past any plane in the solid but gives no information about the time dependence of the vacancy flow. The time dependence is contained in the *Fick's* second law. Considering only vacancy flow in *x*-direction, *Fick's* second law is expressed as:

$$\left(\frac{dC_v}{dt}\right)_x = \frac{d}{dx}\cdot\left[D_v\cdot\left(\frac{dC_v}{dx}\right)_t\right] \qquad (5\text{-}2)$$

If the variation of the vacancy diffusion coefficient D_v with the vacancy concentration C_v is ignored, then *Eq. (5-2)* simplifies to:

$$\left(\frac{dC_v}{dt}\right)_x = D_v\cdot\left(\frac{d^2C_v}{dx^2}\right)_t \qquad (5\text{-}3)$$

The term (d^2C_v/dx^2) graphically represents the *curvature* of a C_v versus x plot.

A crystal has an equilibrium concentration of vacancies and this can be calculated from the *Gibbs* free energy of vacancy concentration. The crystal will be in its most stable state when its *Gibbs* free energy is at minimum, at a given volume and temperature. The number of vacancies corresponding to the minimum *Gibbs* free energy will then be the equilibrium number of vacancies, which can be expressed in the form [31]:

$$C_v^e = \exp\left(\frac{\Delta S}{R}\right)\cdot\exp\left(-\frac{Q_f}{RT}\right) \qquad (5\text{-}4)$$

The first term at the right of the above expression is a constant. Its value is approximately 3 and is independent of the temperature T [31]. The parameter Q_f in the second term is also known as the *activation energy for vacancy formation. Eq. (5-4)* can thus be simplified to:

$$C_v^e \approx 3\cdot exp\left(-\frac{Q_f}{RT}\right) \qquad (5\text{-}5)$$

5-3 Similarity between Vacancy Flow and Heat Flow by Conduction

The equations describing a vacancy flow process are similar to those describing heat flow by conduction. The vacancy flow is driven by vacancy concentration gradient within the crystal whereas heat conduction is driven by a temperature gradient in the medium. During steady-state heat conduction, temperature T and the heat flux $\dot{q}_{cond}$ remain unchanged with time. For a given temperature gradient across the medium, the rate of heat conduction is given by *Fourier's* law. For one-dimensional steady-state conduction in x-direction, *Fourier's* law states that:

$$\dot{q}_{cond} = -k \cdot \frac{dT}{dx} \qquad (W/m^2) \qquad (5\text{-}6)$$

where k is a proportionality constant called *thermal conductivity*, and (dT/dx) is temperature gradient. The minus sign in *Eq. (5-6)* indicates that heat flows by conduction in the direction of decreasing temperature. Comparing *Eq. (5-1)* and *Eq. (5-6)* term by term, one can see the obvious similarity between *steady state* one-dimensional parameters of vacancy flow process and those for conduction heat flow, which are summarized in **Table 5-1.**

In one-dimensional *transient* heat conduction, temperature T normally varies with time t and the position x. For a one-dimensional heat flow in x-direction, the *transient* heat conduction equation can be expressed as:

$$\rho C \cdot \left(\frac{dT}{dt}\right) = \frac{d}{dx} \cdot \left(k \cdot \frac{dT}{dx}\right) \qquad (5\text{-}7)$$

where ρ is *mass density* (kg/m^3) and C is *specific heat* ($J/kg\ K$) of the medium. If the thermal conductivity k does not change with position x, *Eq. (5-7)* simplifies to,

$$\rho C \cdot \left(\frac{dT}{dt}\right) = k \cdot \left(\frac{d^2T}{dx^2}\right)$$

or,
$$\frac{dT}{dt} = \frac{k}{\rho C} \cdot \left(\frac{d^2T}{dx^2}\right) \qquad (5\text{-}8)$$

where parameter ($k/\rho C$) is known as *thermal diffusivity*, denoted as $\alpha (m^2/s)$.

Table 5-1 A summary of a similarity between vacancy flow and heat flow by conduction, for *one-dimensional steady-state* condition.

Vacancy Flow			Heat Conduction		
Vacancy flux	J_v	$\left(\frac{m^3}{m^2 s}\right)$	Heat flux	q_{cond}	$\left(\frac{J}{m^2 s}\right)$
Vacancy diffusivity	D_v	$\left(\frac{m^3}{m \cdot s}\right)$	Thermal conductivity	k	$\left(\frac{J}{m \cdot s \cdot K}\right)$
Vacancy concentration gradient	$\left(\frac{dC_v}{dx}\right)$	$\left(\frac{m^3/m^3}{m}\right)$	Temperature gradient	$\left(\frac{dT}{dx}\right)$	$\left(\frac{K}{m}\right)$

Comparing *Eq. (5-3)* and *Eq. (5-8)*, it can be seen that the vacancy diffusivity, D_v (m^2/s) is similar to the thermal diffusivity, α (m^2/s), i.e.

$$D_v \equiv \frac{k}{\rho \cdot C} \qquad (m^2/s) \qquad (5\text{-}9)$$

For the vacancy flow process, ρ is the *volume fraction* (1 m^3/m^3) of the vacancy and C is *volumetric dilatation* (1 m^3/m^3). It is a measure of how much the volume of a crystal increases or decreases when 1 vacancy is added or taken out from it. **Table 5-2** summarizes the similarity between the vacancy flow and heat flow by conduction for *one-dimensional transient* flow condition.

Table 5-2 A summary of the similarity between vacancy flow and heat flow by conduction, for *one-dimensional transient-state* condition.

Vacancy Flow			Heat Conduction		
Vacancy concentration rate	$\left(\frac{dC_v}{dt}\right)$	$\left(\frac{m^3}{m^3 s}\right)$	Rate of Temperature change	$\left(\frac{dT}{dt}\right)$	$\left(\frac{K}{s}\right)$
Vacancy diffusivity	D_v	$\left(\frac{m^3}{m \cdot s}\right)$	Thermal diffusivity	$\left(\frac{k}{\rho C}\right)$	$\left(\frac{m^3}{m \cdot s}\right)$
Curvature of Vacancy concentration plot	$\left(\frac{d^2 C_v}{dx^2}\right)$	$\left(\frac{m^3/m^3}{m}\right)$	Curvature of Temperature plot	$\left(\frac{d^2 T}{dx^2}\right)$	$\left(\frac{K}{m}\right)$

5-4 Classical Model of *Nabarro-Herring* Creep

Nabarro-Herring creep is accomplished solely by the diffusional mass transport mechanism through the lattice of a crystal, which dominates creep at low stresses and high temperatures, typically greater than $0.5\ T_m$, where T_m is the absolute melting temperature. A detailed description of the *Nabarro-Herring* creep is facilitated by considering how this process is accomplished in a *crystalline* material, as illustrated in **Fig. 5-4.**

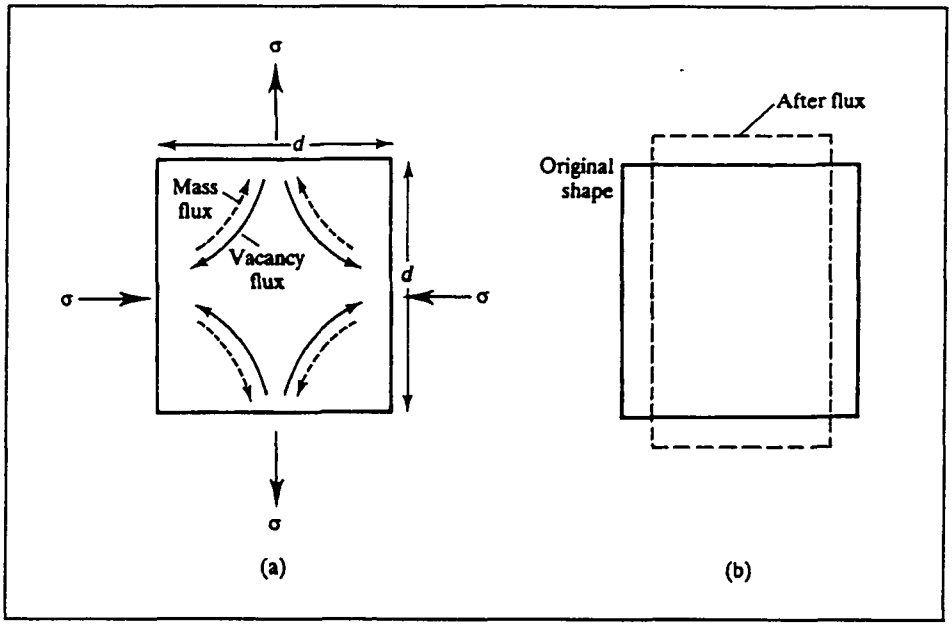


Fig. 5-4 A schematic illustration of classical *Nabarro-Herring* creep model. (a) The applied stresses and the direction of flow of mass and the vacancies. (b) The shape change of the crystal as a result of the diffusive mass and vacancy flow.

The grain shown in *Fig. 5-4(a)* can be considered either as an isolated single crystal or as an individual grain within a polycrystal. It is assumed that the lateral sides of the crystal are subjected to a compressive stress, and the

horizontal sides to a tensile stress of the same magnitude. The applied stresses alter the atomic volume in these regions; it is increased in the tensile region and decreased in the region under compression. As a result, the effective activation energy for vacancy formation is modified by $\pm\sigma\Omega$, where Ω is the atomic volume and the $\pm$ signs refer to compressive and tension regions, respectively. Thus, the fractional vacancy concentration in the tensile and compressively stressed regions are given as [32]:

$$C_v^T \cong 3 \cdot \exp(-\frac{Q_f}{kT}) \cdot \exp(\frac{\sigma\Omega}{kT}) \qquad (5\text{-}10)$$

$$C_v^C \cong 3 \cdot \exp(-\frac{Q_f}{kT}) \cdot \exp(-\frac{\sigma\Omega}{kT}) \qquad (5\text{-}11)$$

where Q_f is the *vacancy-formation energy*. The convention that $\sigma > 0$ is being used in the above expressions and the negative sign in *Eq. (5-11)* is the result of the compressive stress. Provided that the grain boundary is an ideal *source* and *sink* for vacancies, the vacancy concentrations given by *Eq. (5-10)* and *Eq. (5-11)* will be maintained at the horizontal and lateral surfaces of the grain.

The difference in the vacancy concentration between the adjacent faces of the grain creates a *gradient* of vacancy concentration. At high temperatures, this drives a net *flux* of vacancy from the tensile region to the compressively stressed region. This is equivalent to a *net flux* of mass in the opposite direction. The diffusive flow of mass and vacancy result in a change of the grain's shape, as shown in *Fig. 5-4(b)*. The grain elongates in the tensile axis direction and

contracts in the compressive axis direction. In other words, *creep deformation* has occurred. The *steady state* creep rate can be estimated using *Fick's* first law given by *Eq. (5-1)*, in which the vacancy diffusion coefficient D_v can be determined using an expression [32],

$$D_v = D_{ov} \exp(\frac{-Q_m}{kT}) \tag{5-12}$$

where D_{ov} is a *pre-exponential constant*, Q_m is the *activation energy of vacancy motion*, k is *Boltzmann's constant* and T is the absolute temperature. Parameter dx in *Eq. (5-1)* can be considered as a *characteristic diffusion distance*, which is proportional to the grain size, d. The vacancy concentration difference, dC_v can be obtained by taking the difference between the expressions of *Eq. (5-10) and Eq. (5-11)*.

A detail derivation for the expression of the steady state *Nabarro-Herring* creep strain rate, $\dot{\varepsilon}_{NH}$ can be found in *Courtney* [32]. It can be shown that,

$$\dot{\varepsilon}_{NH} = A_{NH} \cdot (\frac{D_L}{d^2}) \cdot (\frac{\sigma\Omega}{kT}) \tag{5-13}$$

where A_{NH} is a geometrical factor equals to 10, d is grain size, and D_L is *lattice self-diffusion coefficient* given by the expression,

$$D_L \equiv D_{ov} \exp\left[-\frac{(Q_f + Q_m)}{kT}\right] \tag{5-14}$$

It has to be emphasized that a geometrical aspect of the crystal has been ignored in the expression for the steady-state *Nabarro-Herring* creep strain rate, $\dot{\varepsilon}_{NH}$ [32].

As a result, the deformed shape of the crystal shown in *Fig. 5-4(b)* is somewhat questionable, especially for a small structure comprising of a single grain. The expression for the steady state creep strain rate of *Eq. (5-14)* would not adequately describe the resulting deformed shape of the crystal. The length of the diffusion path would affect the volume of the atoms being transported. The diffusion path near the corner is much shorter than that near the center of the crystal. Thus, the deformation near the corners of the top surface of the crystal would be more significant than that at the central section. Accordingly, the steady-state creep strain rate at the center of the top surface would be somewhat less than that near the corners.

5-5 Modeling of *Nabarro-Herring* Creep Deformation

A finite element procedure for modeling the classical *Nabarro-Herring* creep deformation in a 1 μm square copper grain, using MARC/Mentat finite element software has been described by *Wu* [14]. The grain was subjected to biaxial normal stresses of ± 10 MPa, at an elevated temperature of 800 °C. **Fig. 5-5** illustrates the steps used in the modeling procedure, which are summarized below:

1. Finite element (FE) models representing the Cu grain were constructed using isoparametric 4-node quadrilateral elements. The models were discretized (or subdivided) into 10 x 10 divisions.

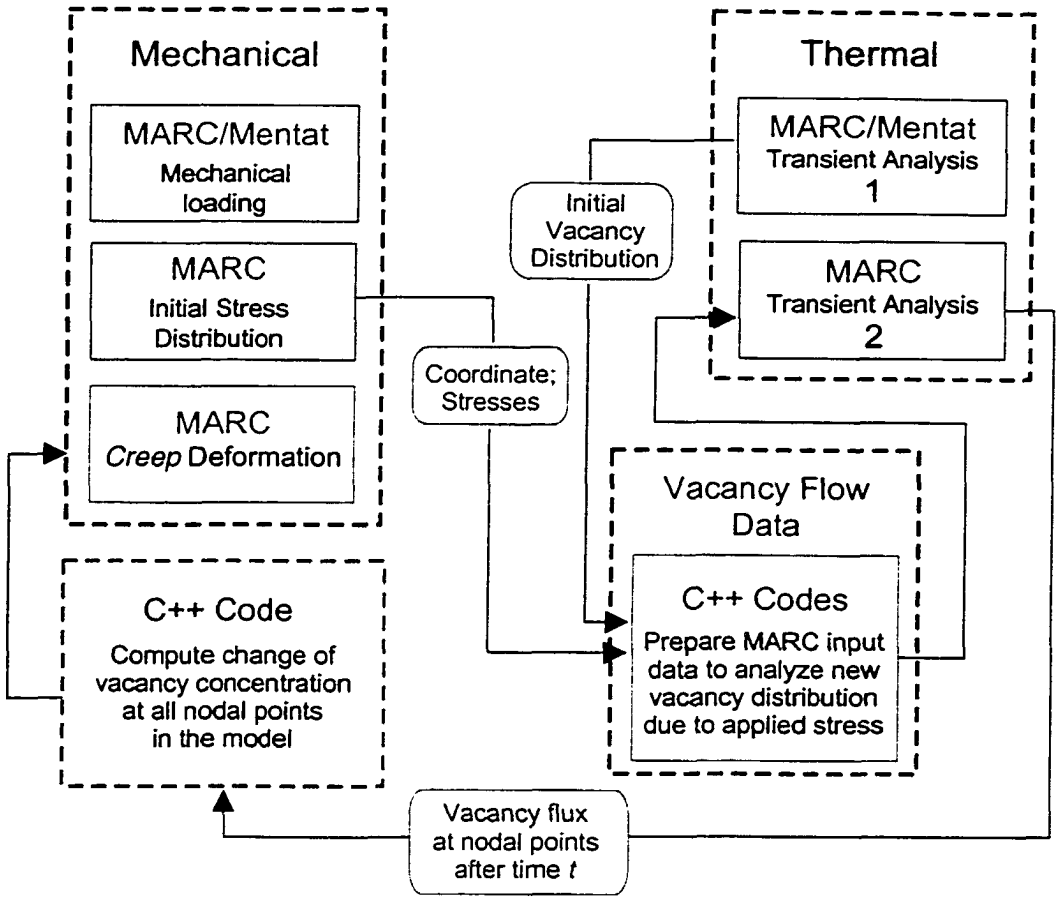


Fig. 5-5 Finite element procedure proposed by *Wu* [14] for modeling the *Nabarro-Herring* creep phenomena in a copper grain at 800 °C.

2. A *linear elastic* mechanical analysis was carried out to simulate the mechanical loading on the grain and to obtain the initial stress distribution in the grain, which was used to compute the initial distribution of vacancy concentration in the grain. **Fig. 5-6** shows the finite element model and the prescribed mechanical boundary conditions for the linear elastic analysis.

3. A *diffusive* vacancy flow analysis was performed using a *transient* heat transfer analysis function of the finite element software, to simulate the *Nabarro-Herring* creep phenomenon.

4. The *new* vacancy concentration at the nodes along the outer boundaries of the grain were then computed based on the steady-state *flux* (in *J/s*) at the nodes, and used to produce the dilatation of the grain, which represented the creep deformation of the grain. The deformed shape of the grain due to creep is shown in **Fig. 5-7.**

5. The *steady state* creep strain rate was computed based on the *y*-displacement of a node at the top surface of the grain.

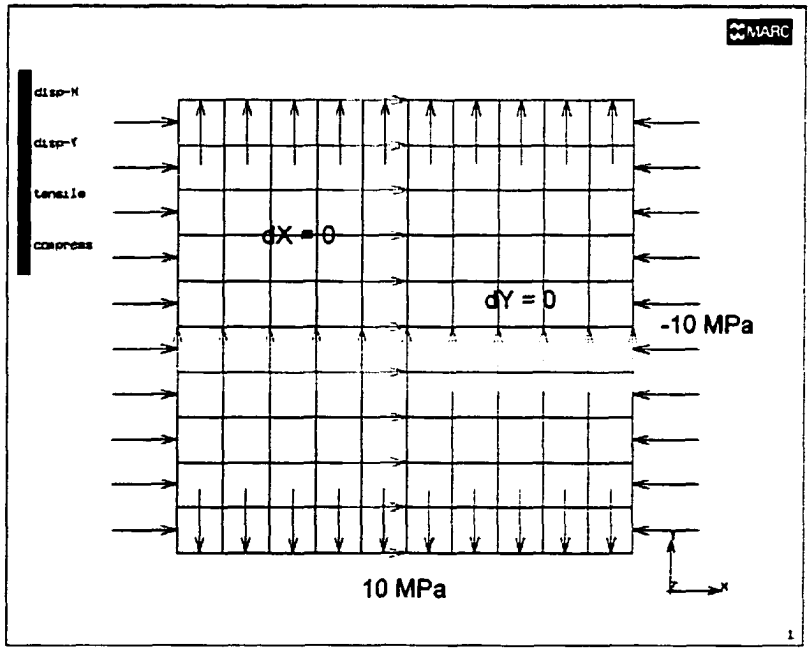


Fig. 5-6 Finite element model of 1 μm square copper grain, discretized into 10 x 10 divisions. Mechanical boundary conditions are shown. (Adapted from [14]).

It can be seen from **Fig. 5-7** that the creep deformation at the corners of the copper grain is somewhat inconsistent with the prediction by the classical *Nabarro-Herring* model. It was shown that the *steady state* creep strain rate at the middle of the top surface is $8.920 \times 10^{-7}\ s^{-1}$ [14].

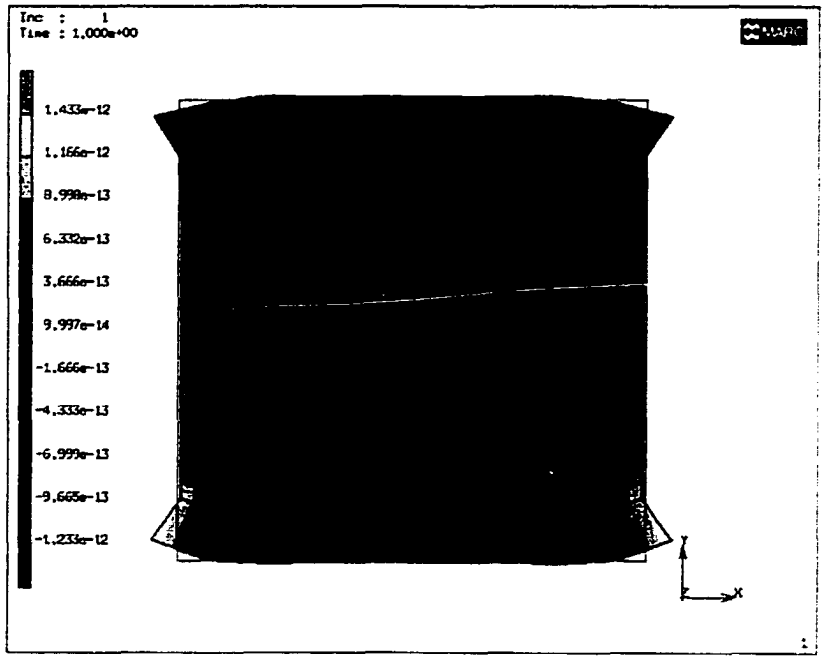


Fig. 5-7 The deformed shape of the copper grain due to vacancy flow creep. Note that the deformation at the corners is somewhat inconsistent with the prediction of the classical *Nabarro-Herring* model. (Adapted from [14]).

In this study, the previously proposed finite element procedure was re-evaluated and modifications were made to improve its overall performance. The steps involved in the new finite element procedure are given in a flowchart diagram shown in **Fig. 5-8.** The steps are summarized as follows.

1. Construct finite element (FE) models of 1 μm square copper grain using isoparametric 4-node quadrilateral element, and discretized the model into 50 x 50 divisions to achieve a better accuracy of the simulation results.

2. Carry out a plane strain *linear elastic* mechanical analysis to simulate the mechanical loading and to obtain the elastic deformation of the copper grain.

3. Perform a *diffusive* vacancy flow analysis using *transient* heat transfer analysis function of the finite element software to simulate the *Nabarro-Herring* creep.

4. Compute the x and y displacements at all the nodes based on the steady state *flux components* (in $J/s\ m^2$), acquired at the end of the vacancy flow analysis. Use the nodal displacements to predict the creep deformation of the grain and to estimate the *steady state* creep strain rate at the boundaries, using an expression

$$\dot{\varepsilon}_y = \left(\frac{2 \cdot \Delta y}{L}\right) \cdot \left(\frac{1}{t_{crp}}\right) \quad (s^{-1}) \qquad (5\text{-}15)$$

where Δy is y-displacement at the boundary (μm), L is length of the sides of the grain (1 μm), and t_{crp} is the time (s) required to achieve the steady state vacancy flow condition.

5. Apply the nodal displacements to the elastically deformed grain (obtained in step 1) to produce the overall deformation of the grain.

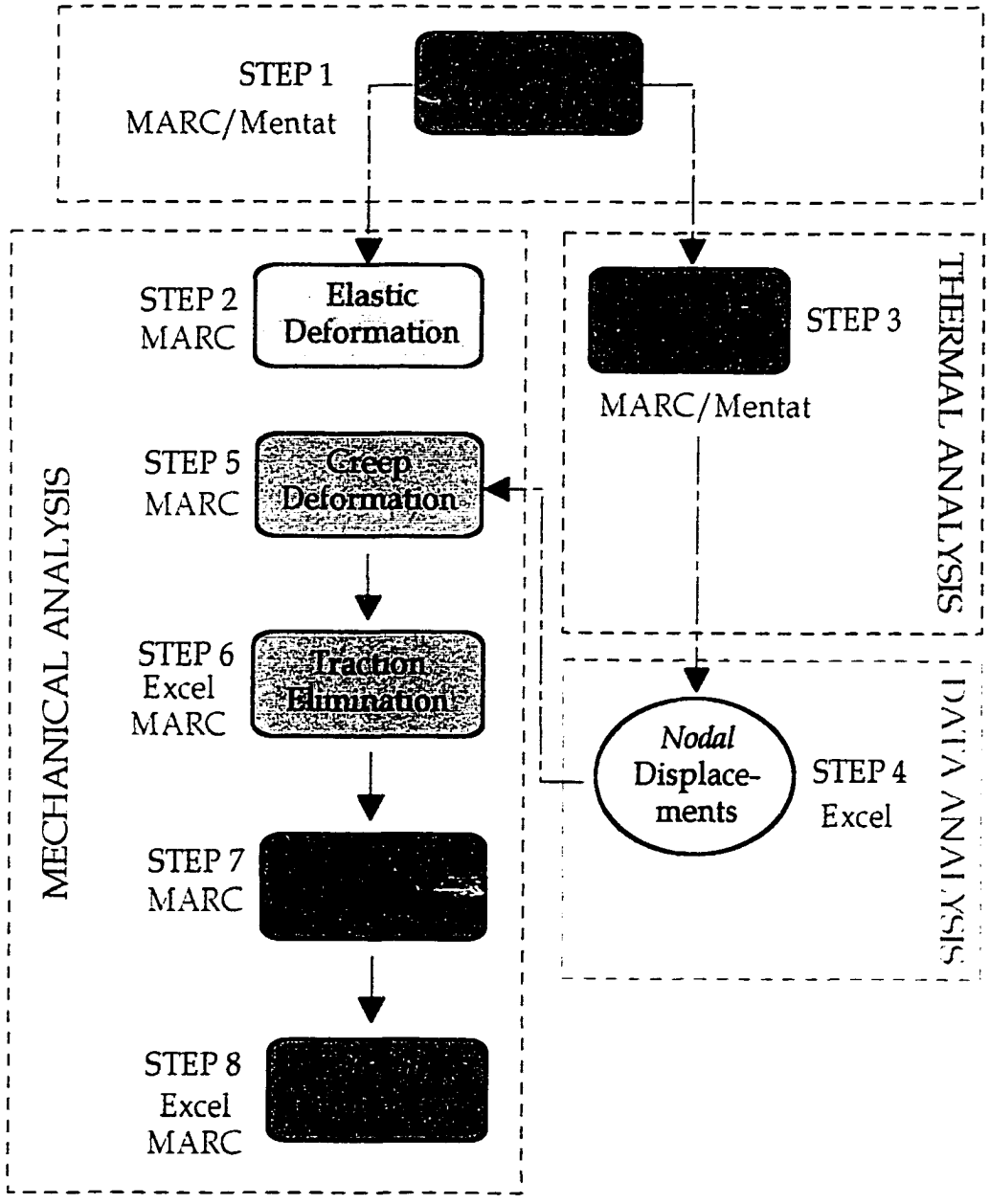


Fig. 5-8 A flowchart diagram showing the steps adopted in the new finite element procedure for modeling the classical *Nabarro-Herring* creep deformation phenomenon.

5-6 Evaluation of *Nabarro-Herring* Creep Parameters

Table 5-3 lists the creep properties of copper and other numerical constants used for evaluating the creep parameters, which are required in the finite element simulation of the *Nabarro-Herring* creep phenomenon.

Table 5-3 Creep properties of copper and other constants used for evaluating the creep parameters required for the simulation of the *Nabarro-Herring* creep phenomenon. (Adapted from [13]).

Parameter (Unit)	Symbol	Value
Absolute temperature (*K*)	T	1073
Atomic volume ($m^3/atom$)	Ω	1.18×10^{-29}
Activation energy of *vacancy formation* (*J/mole*)	Q_f	83.7×10^{-3}
Activation energy of *vacancy motion* (*J/mole*)	Q_m	113.3×10^{-3}
Boltzmann's constant ($J\ K^{-1}$)	k	1.381×10^{-23}
Gas constant ($J\ mole^{-1}\ K^{-1}$)	R	8.314
Grain size (*m*)	d	1×10^{-6}
Lattice *pre-exponential* constant (m^2/s)	D_{oo}	2×10^{-5}

The *equilibrium* vacancy concentration, C_v^e, the instantaneous vacancy concentration on the tensile and compressive faces, C_v^T and C_v^C, were evaluated

using the corresponding expressions in *Eq. (5-5)*, *Eq. (5-10)* and *Eq. (5-11)* respectively. The *vacancy diffusion* coefficient, D_v, and *lattice diffusion* coefficient, D_L were respectively determined using *Eq. (5-12)* and *Eq. (5-14)*. The value of each of these parameters is tabulated in **Table 5-4**.

Table 5-4 The value of *Nabarro-Herring* creep parameters and other constants used for modeling of the creep phenomenon using a finite element procedure.

Parameter (Unit)	Symbol	Value
Equilibrium vacancy concentration (m^3/m^3)	C_v^e	2.5257×10^{-4}
New vacancy concentration on tensile face (m^3/m^3)	C_v^T	2.5459×10^{-4}
New vacancy concentration on compressive face (m^3/m^3)	C_v^C	2.5057×10^{-4}
Vacancy diffusion coefficient (m^2/s)	D_v	6.0993×10^{-11}
Lattice diffusion coefficient (m^2/s)	D_L	5.1350×10^{-15}
Volume fraction (m^3/m^3)	ρ	1
Volumetric dilatation (m^3/m^3)	C	1

The *steady state* creep rate predicted by the classical *Nabarro-Herring* model can be determined using the expression in *Eq. (5-13)*. For an applied normal stress of 10 MPa, *Eq. (5-13)* yields:

$$\dot{\varepsilon}_{NH} \approx 4.089 \times 10^{-4} \quad (s^{-1})$$

5-7 Finite Element Implementation

5-7-1 Construction of Finite Element Models

The finite element models of 1 μm square copper grain were constructed using isoparametric 4-node quadrilateral elements. A 0.5 nm thick boundary element was added to all sides of the models to facilitate future studies on *Coble* creep deformation. The finite element models were discretized (or subdivided) into 50 x 50 divisions to achieve a better accuracy on the finite element results. **Fig. 5-9** shows the finite element mesh of the Cu grain.

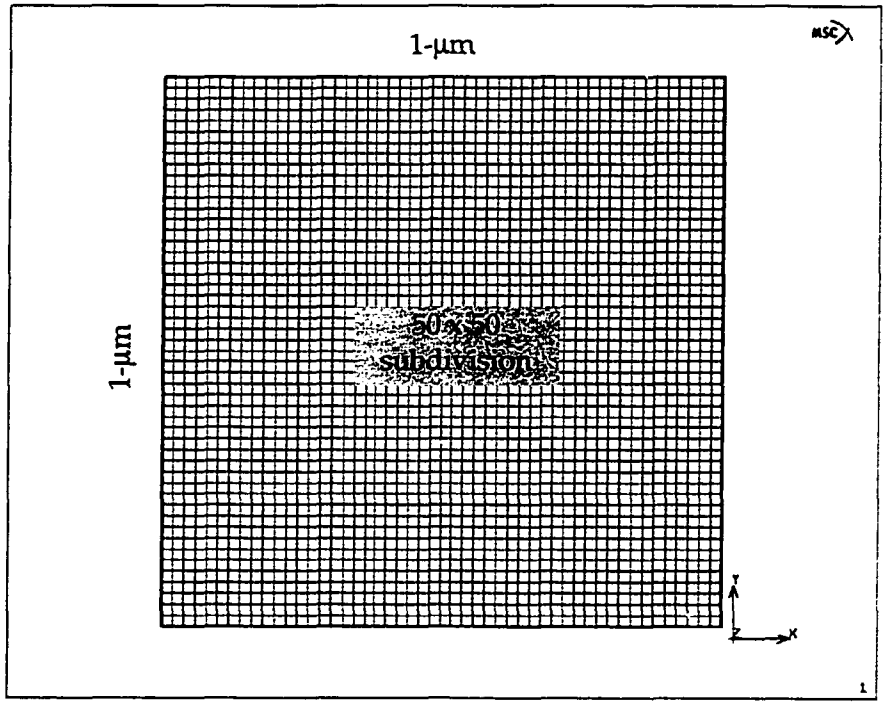


Fig. 5-9 A finite element model of 1 μm square copper grain, constructed using 4-node quadrilateral element, discretized into 50 x 50 divisions.

5-7-2 Linear Elastic Mechanical Analysis

A linear elastic mechanical analysis was performed to simulate the loading on the grain and to produce *elastic* deformation of the grain due to the applied stresses. The following boundary conditions were prescribed on the model for the analysis:

a) The vertical centerline was constrained from x-displacement.

b) The horizontal centerline was fixed in y direction.

c) A compressive *edge load* of 10 MPa was prescribed to the left and right sides and tensile *edge load* of similar magnitude was applied to the top and bottom faces.

Fig. 5-10 shows the finite element model with all boundary conditions prescribed for the linear elastic mechanical analysis. In addition to the above boundary conditions, an equilibrium vacancy concentration (similar to a *fictitious* temperature) of 2.5257×10^{-4} m^3/m^3 was prescribed to the interior of the model to characterize the equilibrium state of the grain at 800 °C.

Next, material properties of copper as shown in **Table 5-5** were prescribed to the mechanical model. To simplify the finite element analysis, the Cu grain was assumed as a homogeneous, isotropic and linear elastic material. The same copper properties were prescribed to the boundary elements.

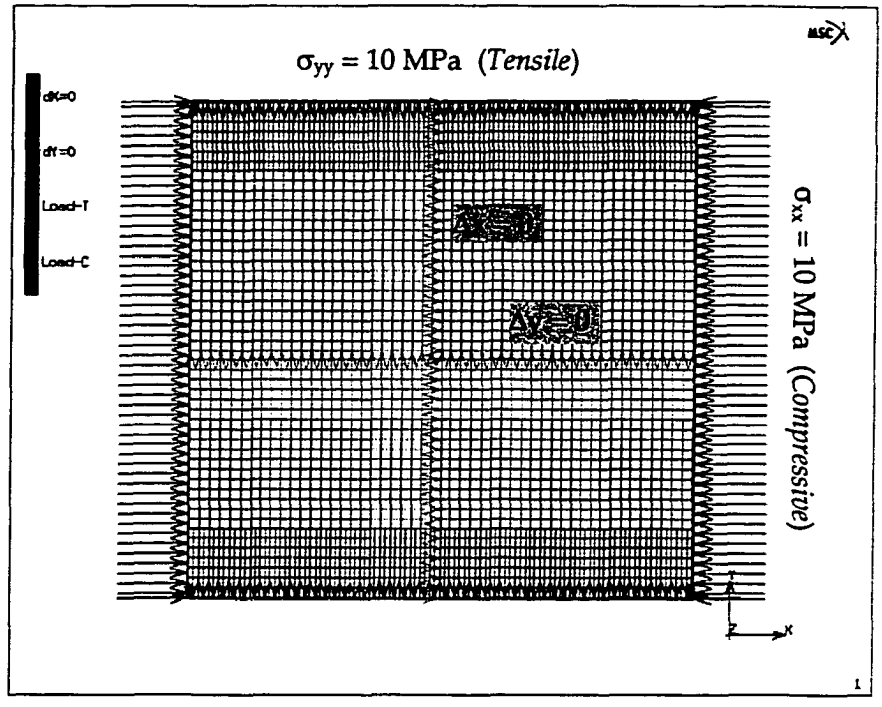


Fig. 5-10 The mechanical model shown with all the boundary conditions prescribed for performing a linear elastic mechanical analysis.

Table 5-5 *Isotropic* mechanical properties of copper prescribed to the mechanical model for performing a linear elastic mechanical analysis.

Property	Symbol	Value
Young's Modulus (*Pa*)	E	128×10^9
Poisson ratio	ν	0.36
Mass density (kg/m^3)	ρ	1

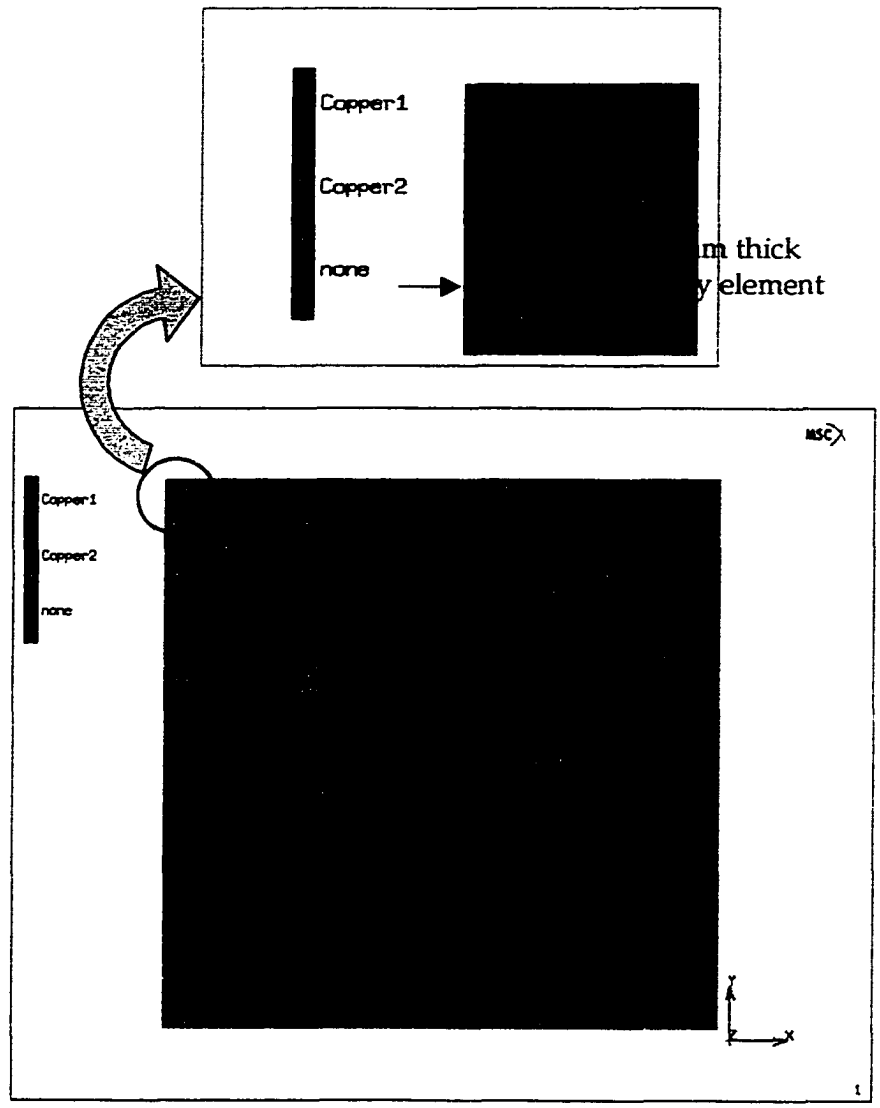


Fig 5-11 Isotropic material properties of copper prescribed on the finite element model for linear elastic mechanical analysis. A smaller picture at the top shows a close-up view of the top left corner of the grain.

Fig. 5-11 shows the mechanical model with the prescribed isotropic material properties of copper for performing the mechanical analysis. A close up view of the top left corner portion of the model is shown in a smaller picture at the top.

5-7-3 Diffusive Vacancy Flow Analysis

A *diffusive* vacancy flow analysis was performed to simulate the Nabarro-Herring creep phenomenon using *transient* heat transfer analysis function of MARC/Mentat finite element software. The following vacancy boundary conditions were prescribed on the finite element model for the analysis:

a) A vacancy concentration of 2.5057×10^{-4} m^3/m^3 was prescribed on the left and right faces of the grain.

b) A vacancy concentration of 2.5459×10^{-4} m^3/m^3 was specified on the top and bottom faces of the grain.

c) An equilibrium vacancy concentration of 2.5257×10^{-4} m^3/m^3 was prescribed on the four corners of the grain (the corner nodes were assumed at zero stress).

d) An equilibrium vacancy concentration of 2.5257×10^{-4} m^3/m^3 was prescribed on the entire interior of the grain to represent the initial equilibrium state of the grain prior to creep.

The boundaries of the grain were assumed as the infinite *sources* and *sinks* for vacancies, thus the vacancy concentrations at the boundaries were held constant during the entire diffusive vacancy flow analysis. The vacancy concentration at the interior was allowed to change with time. **Fig. 5-12** shows the finite element model with the prescribed vacancy boundary conditions.

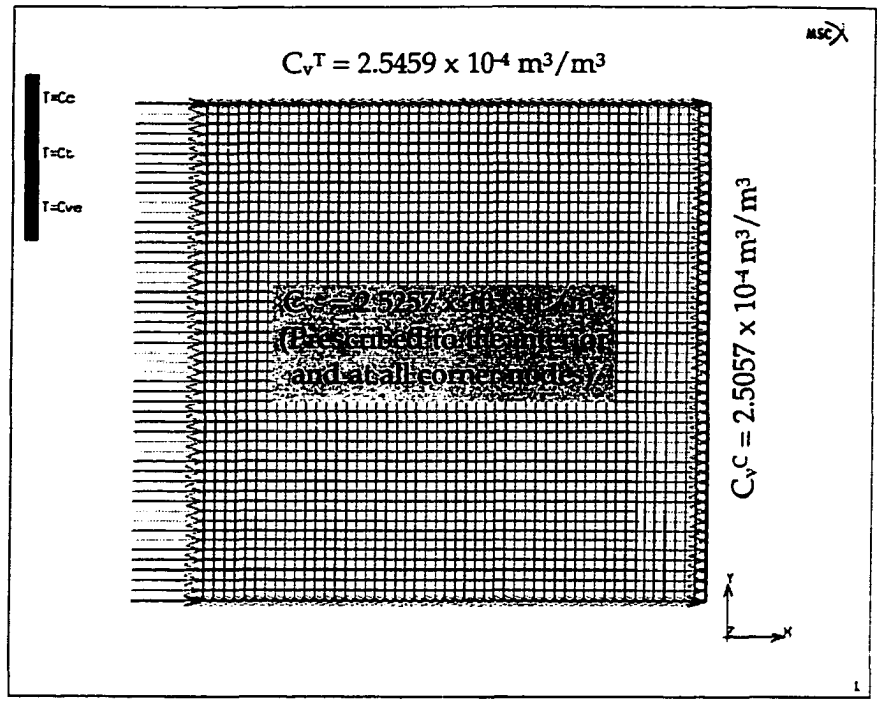


Fig. 5-12 Vacancy boundary conditions prescribed to the finite element model for performing diffusive vacancy flow analysis.

Table 5-6 Vacancy flow parameters prescribed to the finite element model for performing the diffusive vacancy flow analysis.

Property	Symbol	Value
Vacancy diffusivity (m^2/s)	D_v	6.0993×10^{-11}
Volumetric dilatation (m^3/m^3)	C	1
Volume fraction (m^3/m^3)	ρ	1

Next, vacancy flow parameters for copper (similar to *isotropic* heat transfer material properties) were prescribed, in which vacancy diffusivity, D_v (similar to thermal conductivity, k), volumetric dilatation, C (similar to specific heat, C) and volume fraction of vacancy, ρ (similar to mass density, ρ) were applied to all the elements. **Table 5-6** lists the value of these parameters. The *diffusive* vacancy flow analysis was carried out for a total time of 6×10^{-4} seconds to ensure that a *steady state* vacancy flow condition is achieved at the end of the analysis.

5-8 Results and Discussion

5-8-1 Linear Elastic Mechanical Analysis

Fig. 5-13 shows the elastic deformation of the grain resulting from the applied stresses on the boundaries, magnified by a factor of 1:500. The undeformed shape of the grain is indicated by the square shape colored pink. As one would expect, the grain experiences a uniform deformation in the direction of the applied stresses. As indicated in the figure, the uniform y-displacement at the top and bottom faces of the grain is 5.3284×10^{-11} m, resulting in an elastic strain of 1.065×10^{-4}.

5-8-2 Diffusive Vacancy Flow Analysis

Fig 5-14 shows the variation of vacancy *flux*, Q with creep time, t_c, at a node in the middle of the top surface, indicating that a steady state vacancy flow condition was attained after 6×10^{-4} seconds.

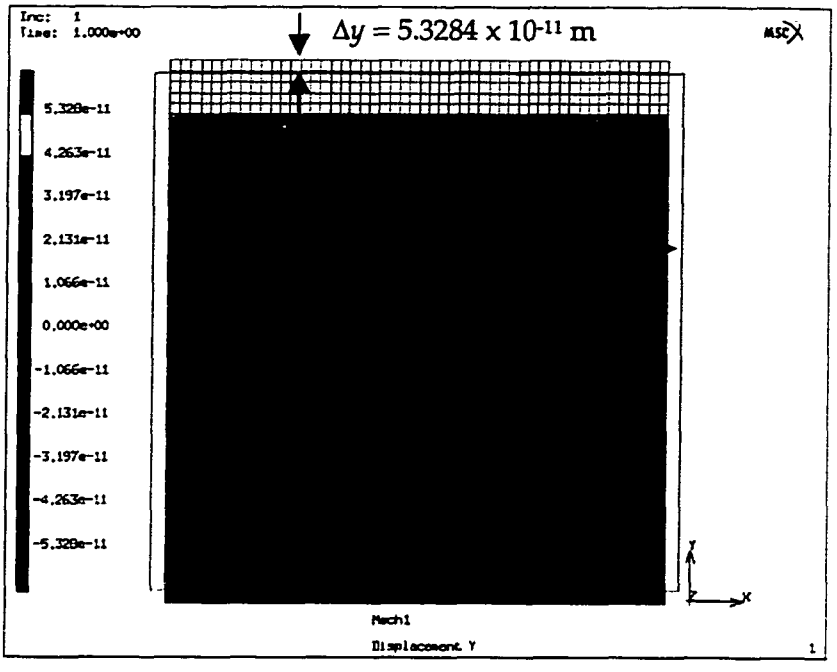


Fig. 5-13 Elastic deformation of the grain due to the applied stresses on the boundaries, magnified by a factor of 1:500.

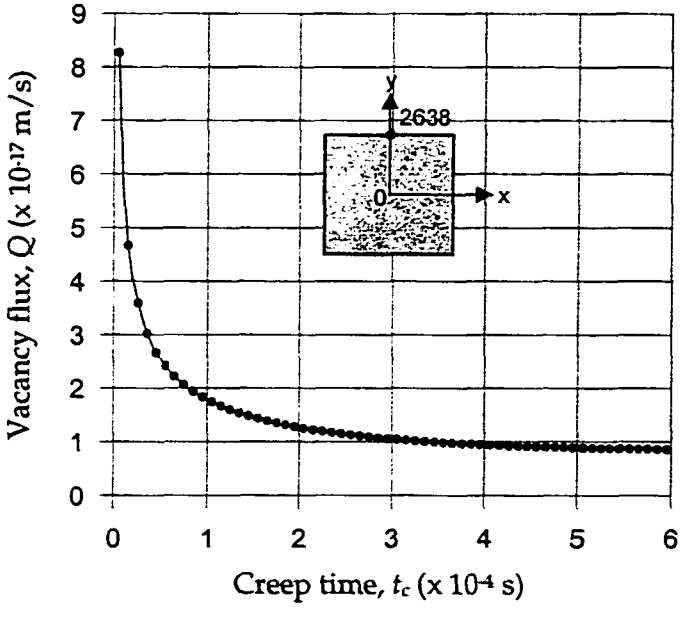
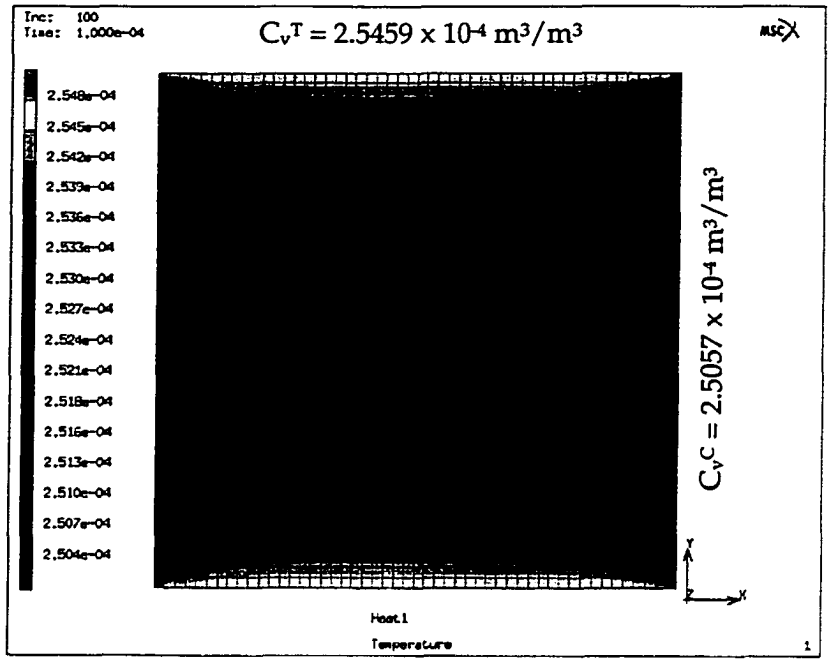


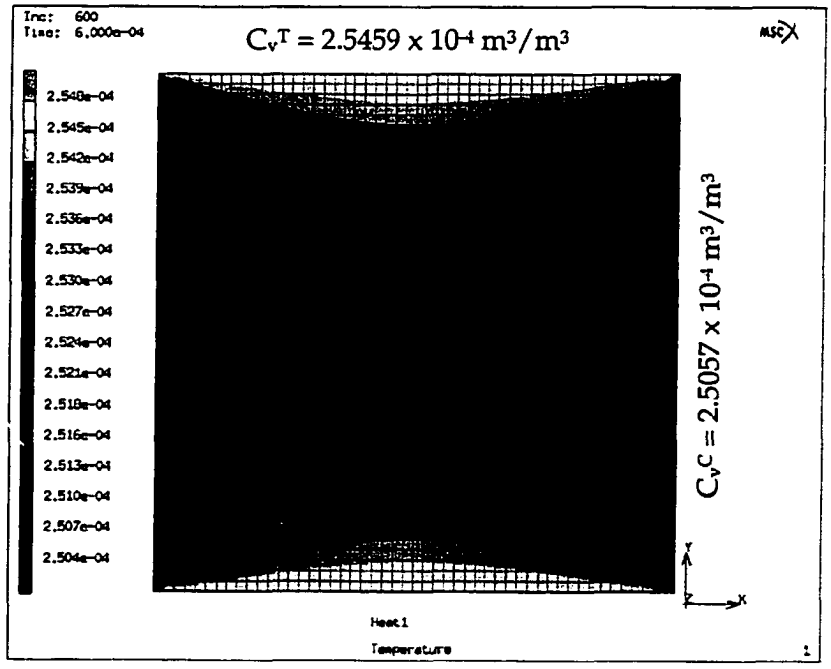
Fig. 5-14 Variation of vacancy *flux* at the middle of the top surface with creep time.

Fig. 5-15 shows new distribution of vacancy concentration in the grain. *Fig. 5-15(a)* shows the vacancy concentration distribution after 1×10^{-4} s while *Fig. 5-15(b)* shows that after 6×10^{-4} s. It can be observed that the vacancy distribution has not yet fully developed after 1×10^{-4} s, indicating that the vacancy flow process is still in a *transient* state. On the other hand, the vacancy concentration distribution in *Fig. 5-15(b)* is fully developed after 6×10^{-4} s. The same vacancy distribution profile was obtained even when the creep time was further extended to 10×10^{-4} seconds.

The vacancy concentration gradient that was established between two adjacent faces of the grain drives a flow of vacancy flux from the faces having high vacancy concentration to those having lower vacancy concentration. The resultant vacancy *flux*, Q will always act *normal* to the lines of constant vacancy concentration. As illustrated in **Fig. 5-16,** vacancies flow from the left portion of the top surface to the upper part of the left surface (indicated by the yellow arrows). The vacancy flow in one direction is complemented by a flow of matter in the opposite direction, as indicated by the blue arrows in the figure. As a result of this process, each node in the finite element model undergoes displacements in x and y directions, and consequently the grain undergoes a deformation due to creep by vacancy flow mechanism.



(a)



(b)

Fig. 5-15 The new distribution of vacancy concentration in the finite element model (*a*) after 1×10^{-4} s and (*b*) after 6×10^{-4} s of the diffusive vacancy flow analysis.

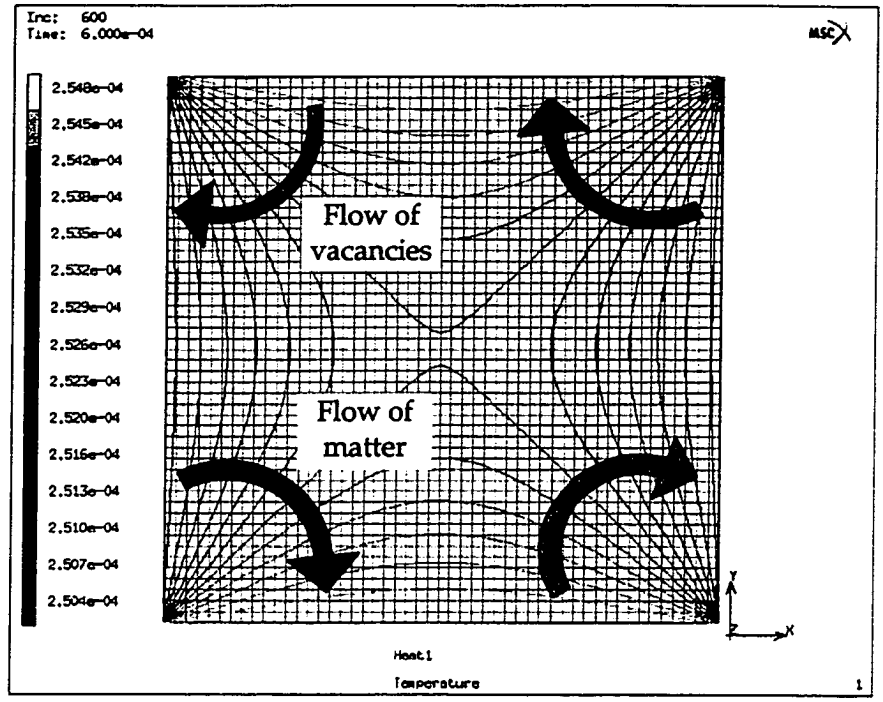


Fig. 5-16 Profile of lines of constant vacancy concentration at the steady state condition. The yellow arrows indicate the direction of vacancy flow while the blue arrows indicate that of matter flow, during the creep process.

5-8-3 Creep Deformation of the Grain

The *steady state* components of vacancy *flux* at all the nodes were manually acquired at the end of the diffusive vacancy flow analysis. The flux components have a unit of *m/s* and therefore are similar to the components of velocity at the nodes. This allows the displacements (in x and y directions) at each node to be determined, since the time taken to attain the steady state is known. For example, the x-component of the vacancy flux at the middle of the left surface is q_x = -5.1911 x 10^{-10} m/s. Therefore, this node undergoes an x-displacement of:

$$\Delta x = q_x \times t_c \times (-1) = 3.1146 \times 10^{-13} \text{ m.}$$

Note that a multiplication factor of (–1) has been used in the above computation because matter flows in the opposite direction to the vacancies. The same procedure was used to compute the nodal displacements at all the nodes.

The nodal displacements were utilized to predict the creep deformation of the grain. First, the displacements were applied to the corresponding nodes in a new finite element model. Then, a linear elastic mechanical analysis was performed to produce the creep deformation of the grain. **Fig. 5-17** shows the deformed shape of the grain, magnified by a factor of 1:500. It can be observed that the *y*-displacement distribution is symmetric about the horizontal centerline of the grain. This observation verifies that the use of transient heat transfer analysis function of MARC finite element software to simulate the diffusive vacancy flow process is a valid approach. It can also be noticed that the corners of the grain are somewhat distorted as a result of the magnification process. A close-up view of the deformation at the top left corner of the grain is shown in **Fig. 5-18** with a 1:1 magnification factor. The lines shown in pink color indicate the undeformed shape of the grain. It is clear from the figure that the creep deformation of the grain is in very good agreement with that predicted by the classical *Nabarro-Herring* creep model.

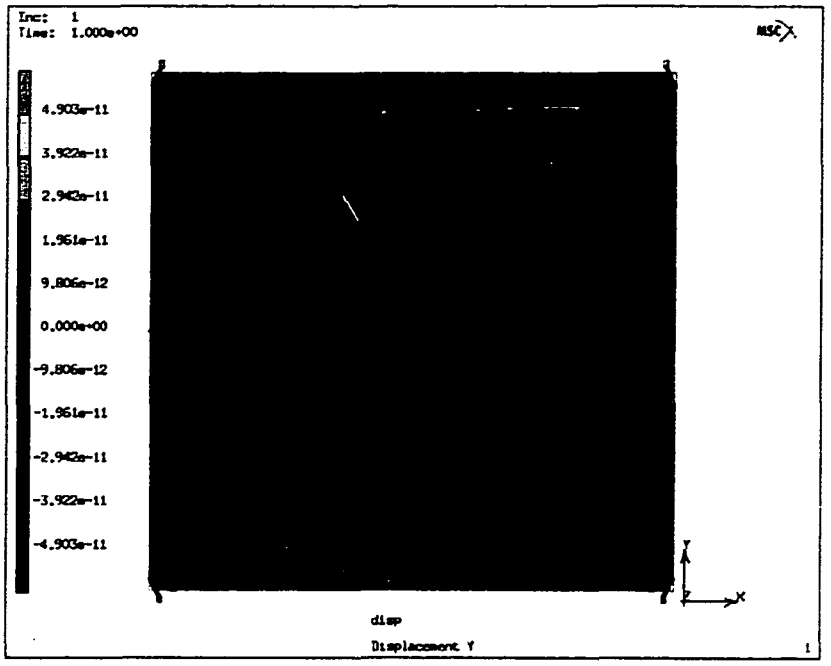


Fig. 5-17 Deformed shape of the grain due to the vacancy flow creep, magnified by a factor of 1:500.

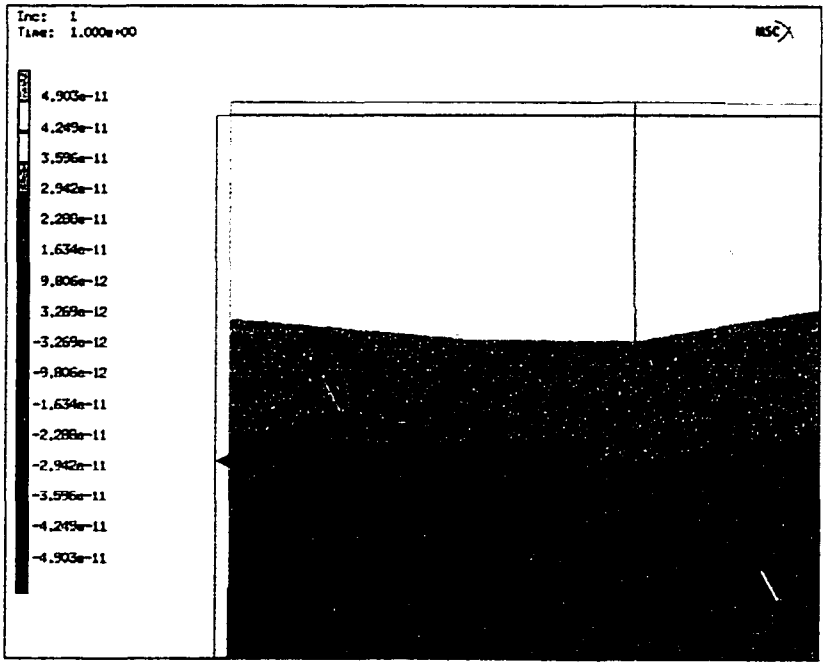


Fig. 5-18 A close-up view of the deformation at the top left corner of the grain.

Fig. 5-19 shows a plot of x-displacement profile along the left face of the grain. The x-displacement at the two corner nodes is unrealistically large, and thus is not shown in the plot.

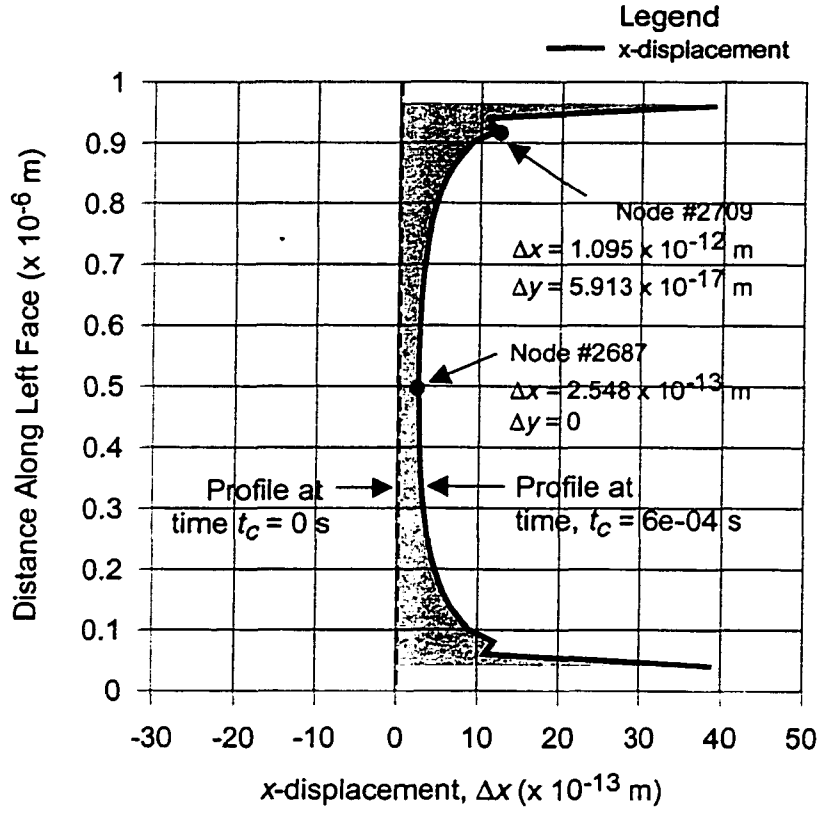


Fig. 5-19 Profile of x-displacement along the left face of the grain. The shaded area represents accumulated amount of matter transported away from the surface, up to the steady state condition.

It can be seen from the figure that the x-displacement is symmetric about the mid-point of the surface. The node in the middle of the surface undergoes the smallest x-displacement of 2.548×10^{-13} m, and zero y-displacement. It can also be observed that the x-displacement increases dramatically in areas close to the top and bottom portion of the surface and the y-displacement in these areas has a

non-zero value. However, the y-displacement component is small and therefore is not expected to affect the resultant of the displacement in these areas.

The fact that the x-displacement is greater in the upper and lower portions of the surface indicates that more material was transported away from these regions during the creep process, compared to that at the middle. This is conceivable since the regions closer to the corners experience much greater vacancy concentration gradient as the distance between the two adjacent faces becomes increasingly shorter. Another words, the regions close to the corners have much shorter *diffusion paths* compared to those near the center of the left face. The node right at the middle of the surface has the longest diffusion path and thus is expected to experience the smallest displacement. The shaded area under the curve represents the accumulated amount of matter that was transported away from the surface, up to the steady state condition. An exactly similar situation was observed on the right face of the model, except that the x-displacement is in the opposite direction.

Fig. 5-20 shows plot of y-displacement profile along the top surface of the grain. It can be seen from the plot that the y-displacement is also symmetrical about the mid-point of the surface. The y-displacement increases in the areas near the left and right corners, which indicates that larger amount of matter was transported into these areas during creep. The shaded area indicates the accumulated amount of material that diffused from the left and right faces.

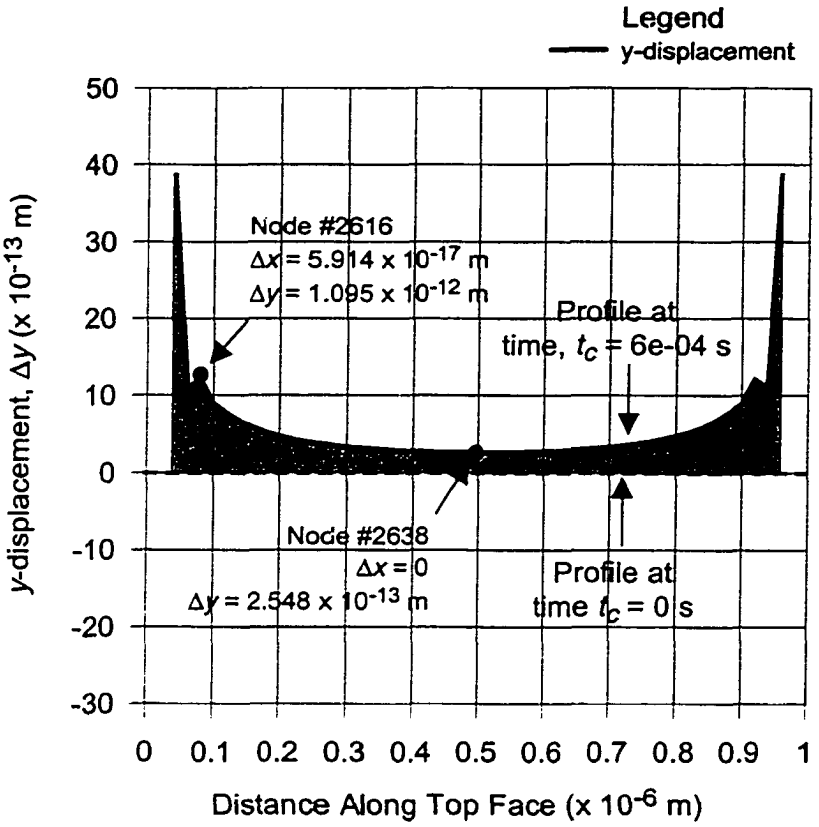


Fig. 5-20 Plot of *y*-displacement profile along the top face of the grain. Note that the shaded area is proportional to the accumulated amount of material that diffused from the top half portion of the left and right faces.

The node at the middle of the surface experiences the smallest *y*-displacement whereas that located at 60 nm away from the top left corner undergoes nearly 4 times greater *y*-displacement. A similar situation was observed at the bottom surface of the grain, except that the *y*-displacement at each node is in the opposite direction.

5-8-4 Effects of Boundary Traction

As described earlier, displacements at the nodes were utilized to produce the deformed shape of the grain due to vacancy flow creep. Since the sides of the grain undergo some displacements, MARC finite element software automatically computed the equivalent *traction* (or reaction forces) required to produce the displacements of the boundaries. As a result, the copper grain was subjected to *additional* applied stresses during the vacancy flow creep. This effect is undesirable and therefore needs to be eliminated, because the initial applied stresses must remain constant during creep.

The elimination of the boundary traction effect can be accomplished using the following procedure:

a) Acquire the boundary traction (or reaction force) data at all nodes along the boundaries of the grain.

b) Apply negative traction of equal magnitude to the corresponding sides of a new finite element model, and then perform a mechanical analysis to produce the deformation due to the *additional* stresses.

c) Subtract the additional deformation from the creep deformation due to vacancy flow obtained earlier, to get the *net* creep deformation of the grain.

The boundary traction data was acquired from the deformed grain and it was found that the average value of the boundary traction on all sides of the grain is on the order of $\pm 1.0 \times 10^{-2}$ N. This produces an *additional* applied stress of approximately ± 10 KPa on the grain. It can be seen that the additional stresses due to the boundary traction are negligibly small (about 0.1%) compared to the initial applied stresses of ± 10 MPa. Therefore, they are not expected to have any significant impact on the creep deformation of the grain. Because of this no further attempt was made to eliminate the effects of the boundary traction. Therefore, the creep deformation of the Cu grain obtained earlier was considered as the *net* creep deformation of the grain due to vacancy flow.

5-8-5 Steady State Creep Strain Rate

The steady state creep strain rate $\dot{\varepsilon}_{FE}$ at the boundaries of the grain was determined using *Eq. (5-15)* based on the *y*-displacement at a node located at the middle of the top surface of the grain. The finite element result was then compared to the prediction by the classical *Nabarro-Herring* creep model, to evaluate the performance of the finite element procedure. The comparison is shown in **Table 5-7**. It can be seen that, the finite element result agrees with the analytical prediction within a factor of two. The difference between the finite element result and that of the analytical model could be because *biaxial* stress state was used in the finite element simulation, whereas *Eq. (5-15)* was formulated based on a *uniaxial* stress condition.

The result of the previously proposed finite element procedure is also shown in the table. It can be seen that the previous result obtained by *Wu* [14] is more than three orders of magnitude lower as compared to the prediction of the *classical* creep model.

Table 5-7 Comparison between the results of finite element simulation and the prediction of the classical *Nabarro-Herring* creep model.

Method	Steady State Creep Strain Rate (s^{-1})
Previously proposed finite element procedure, (Wu [14]).	8.920×10^{-7}
Classical *Nabarro-Herring* creep model.	4.089×10^{-4}
New finite element procedure.	8.547×10^{-4}

Fig. 5-21 shows the variation of creep strain rate with creep time, for the node located at the middle of the top surface. It can be seen from the plot that the creep rate is highest at the beginning of the vacancy flow process, indicating a *transient* state of the vacancy flow. The creep rate then decreases drastically with time until about 0.5×10^{-4} s. Thereafter, the creep rate decays somewhat exponentially with time, up to about 4×10^{-4} s. The creep rate becomes less significantly affected by time after 5×10^{-4} s, an indication of the *steady state* vacancy flow condition.

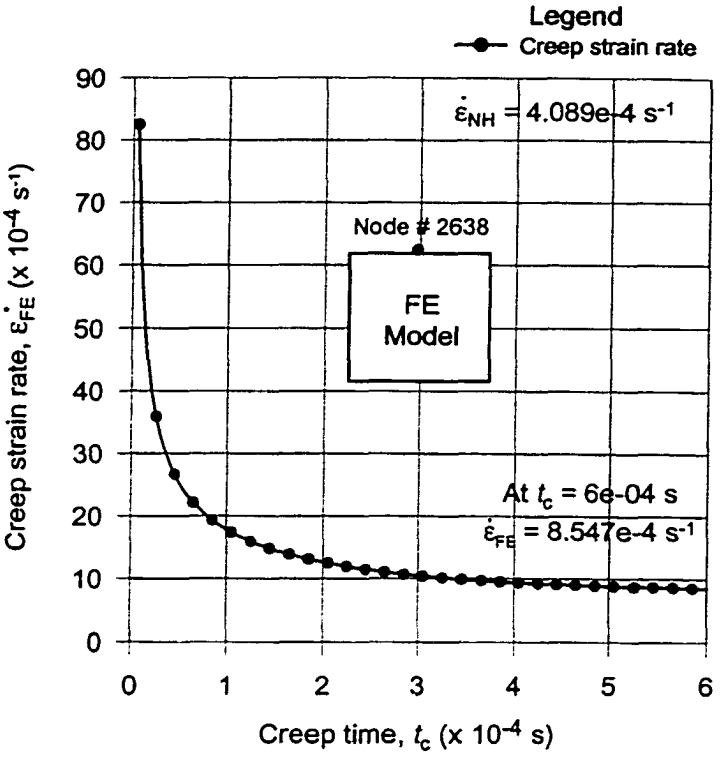


Fig. 5-21 Variation of creep strain rate with the creep time, for the node located at the middle of the top surface.

5-8-6 Optimization of Finite Element Discretization

The finite element models were first discretized into 10 x 10 divisions and the finite element simulation was carried out using to the procedure described earlier and the *steady state* creep strain rate at the middle of the top surface of the grain was determined. Then, the element discretization was further refined to 20 x 20 divisions and 50 x 50 divisions, and the finite element analysis was repeated for each subdivision. The *steady state* creep strain rate obtained for all the element discretization schemes are compared to the result predicted by the classical

Nabarro-Herring model, as shown in **Table 5-8.** It can be seen that, the creep strain rate is strongly affected by the element size, for subdivision less than 20 x 20, which is an undesirable effect. The element size effect on the creep rate becomes insignificantly small when the discretization was further refined from 20 x 20 division to 50 x 50 division. Based on the observed trend, further refinement in the finite element discretization is not expected to significantly improve the result. Moreover, data acquisition, manipulation and analysis will become more cumbersome if the finite element models are discretized into more than 50 x 50 divisions. Therefore, the 50 x 50 discretization schemes have been adopted.

Table 5-8 Comparison between results of various discretization schemes and that predicted by the classical Nabarro-Herring creep model, for a creep time of 5×10^{-4} s.

Discretization	(s^{-1})	(s^{-1})
10 x 10	3.6645×10^{-4}	4.089×10^{-4}
20 x 20	8.5306×10^{-4}	
50 x 50	8.8561×10^{-4}	

5-8-7 Overall Deformation of the Grain

The overall deformation of the Cu grain was obtained by *superimposing* the elastic deformation due to the applied stresses and the *net* creep deformation due to vacancy flow mechanism. **Fig. 5-22** shows the overall deformed shape of the model, magnified by a factor of 1:500. Notice that the deformed shape of the

grain is consistent with the prediction of the analytical model although the corners are somewhat distorted due to the magnification. The undeformed shape of the grain is indicated by the pink colored square shape.

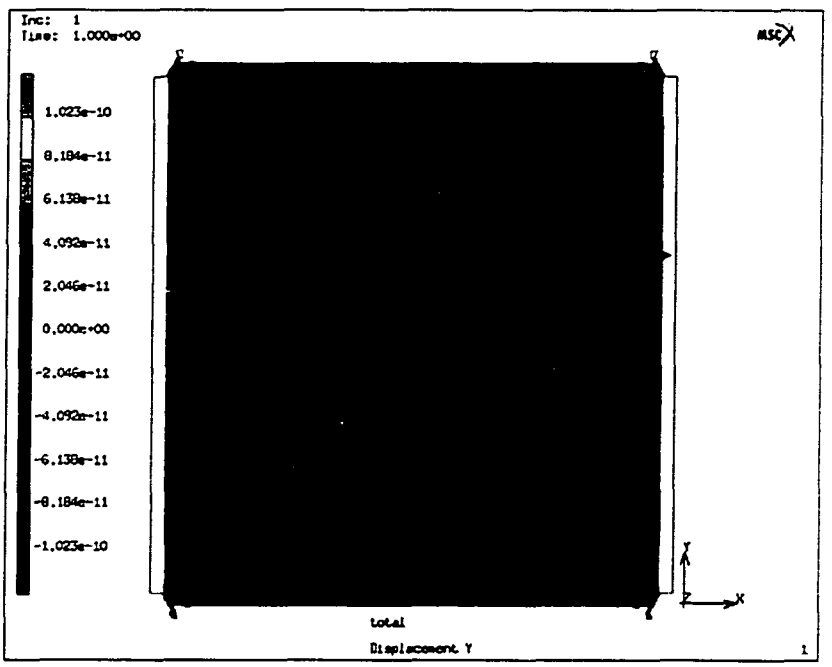


Fig. 5-22 An *overall* deformed shape of the copper grain, magnified by a factor of *1:500*. Note that the corners are somewhat distorted as a result of the magnification process.

Fig. 5-23 shows a plot of *y*-displacement profile along the top surface of the grain. The trend seen in this plot is similar to that shown in *Fig. 5-20*. The *y*-displacement increases in the areas closer to the corners because more material is being transported into this region from the upper portion of the left and right sides during the vacancy flow creep, since the diffusion path is shorter in these regions compared to that in the middle region.

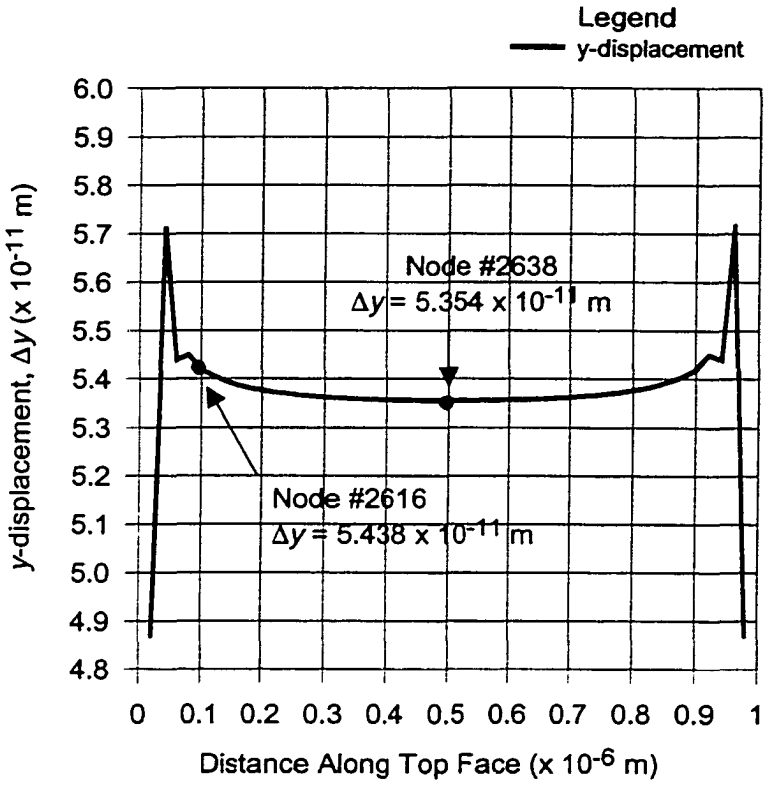


Fig. 5-23 A plot of the overall *y*-displacement profile along the top surface of the grain.

5-9 General Summary

A finite element procedure was used to simulate the classical *Nabarro-Herring* creep deformation phenomenon in a 1 μm square copper grain subjected to biaxial stresses of ± 10 MPa at 800 °C. The previously proposed numerical procedure, which used the new vacancy concentration at the boundaries to predict the creep deformation of the grain, was re-evaluated and modifications were made to improve its performance. The previous result was shown to be

about three orders of magnitude lower than that predicted by the analytical creep model. The new procedure, which used nodal displacements computed based on the components of vacancy flux at all the nodes to predict the creep deformation of the grain, was found to be capable of modeling the *Nabarro-Herring* creep phenomenon satisfactorily. The finite element result agrees with the prediction of the classical *Nabarro-Herring* model within a factor of two.

5-10 Suggestions for Future Work

Although the new finite element procedure is capable of modeling the classical *Nabarro-Herring* creep deformation phenomenon, many improvements can be made on the procedure to enhance its performance and to make it easier to use. Below are some suggestions that can be implemented in the future:

i) At present, the information from the diffusive vacancy flow analysis that are required for predicting the creep deformation of the grain and for estimating the steady state creep strain rate were acquired, manipulated, and processed, manually. The efficiency of the finite element procedure can be greatly improved if these steps can be carried out automatically, for instance using specifically written computer programs in C++ or *Fortran 77* programming languages. Preliminary work on this aspect is now in progress.

ii) The finite element results obtained in this study apply only to a single "loop" analysis. In the future, the analysis can be performed in more than a single loop, so that a more realistic creep behavior of the copper grain can be investigated.

iii) Use the finite element procedure to simulate the classical *Nabarro-Herring* creep deformation phenomenon in more complex grain geometries.

iv) Use the finite element procedures to study creep deformation of copper grain due to vacancy flow along the grain boundary (*Coble* creep mechanism).

Chapter 6

CONCLUSION

An atomic force microscope (AFM) was used to measure thermally-induced deformation of a 1 μm thick single level damascene copper-polyimide interconnect structure as a result of a 25°C-350°C-25°C thermal cycle. Out-of-plane deformation maps of areas of copper and polyimide via structure were generated by subtracting the topographical images obtained before the thermal cycle from the images of the same area, acquired after the thermal cycle. The deformation maps of the copper film areas exhibited evidence of:

a. Sliding at copper grain boundary.
b. Ditching around the copper grain boundary, attributed to *Coble* creep mechanism.
c. Formation of small and larger voids.
d. Interfacial sliding at copper-tantalum interface.
e. Shrinkage of smaller copper grains.

In one Cu film area, sliding at the Cu grain boundary resulted in large extrusion of individual copper grains at isolated areas far away from the Cu-Ta interface. In the other Cu film area, the sliding resulted in elevation and depression of Cu grains as a whole unit and most of them are tilted at some angle relative to the film's plane. In large Cu vias, the grains adjacent to the Cu-

Ta interface were elevated relative to the surrounding polyimide whereas the grains in the middle are depressed. In smaller Cu vias, most of the grains are depressed relative to the polyimide.

Ditching around Cu grain boundary attributed to *Coble* creep mechanism was occasionally observed, but deformation by Cu grain boundary sliding was a more dominant mechanism. The deformation maps of Cu film also show evidence of formation of small voids scattered at some isolated areas, and some larger voids that look like shrinking of some small Cu grains.

Interfacial sliding at the Cu-Ta interface resulted in what may be elastic or inelastic deformation of the polyimide. For all the Cu vias, it is proposed that the polyimide and Ta slid upwards with respect to the Cu by diffusion-accommodated sliding during the heating part of the cycle. This sliding did not completely recover during the cooling cycle resulting in the polyimide appearing to be held up at the Cu-Ta interface. The polyimide vias exhibited a more complex, size dependent Cu-Ta interfacial sliding behavior. The direction of the Cu-Ta sliding, as inferred from the curvature of the polyimide, changed from up to down as the width-to-depth aspect ratio of the vias decreases. This is attributed to an increasing constraint on the out-of-plane expansion of the polyimide as the size of the vias becomes increasingly smaller.

The polyimide undergoes a residual deformation in the areas close to the Cu-Ta interface attributed to the Cu-Ta interfacial sliding. The polyimide around

the Cu vias is depressed farther away from the Cu-Ta interface, attributed to the in-plane deformation of the vias at high temperatures.

A plane strain finite element method was used to simulate the effect of Cu-Ta interfacial sliding on the interfacial and liner plane stresses in a 1 μm thick single level *Benzocyclobutane* (BCB)-copper and SiO_2-copper interconnect structures as a result of heating from 20°C to 400°C, assuming that the structures are stress free at 20°C. The sliding effects were incorporated into the finite element models using a 1 nm thick creep element that was calibrated to match the predictions of a classical diffusion-accommodated sliding model proposed by *Raj & Ashby*. The Cu-Ta sliding causes the shear stress at the interface to relax in exponential decay with time. For a given temperature, the rate of shear stress relaxation in the SiO_2-Cu structure is about 4 times faster than that in the BCB-Cu structure. The direction of the Cu-Ta sliding in the BCB-Cu system is strongly affected by both the Ta liner thickness and the width-to-thickness (w/t) aspect ratio (when the Ta liner is 10 nm thick).

The Cu-Ta sliding has a minor effect on the interfacial shear stresses in the BCB-Cu structure. The sliding causes the interfacial shear stresses in the SiO_2-Cu structure to relax to negligibly small values, for all the w/t ratios considered. The Ta liner plane stresses in the BCB-Cu structure with thin Ta liner and large aspect ratio are strongly affected by the Cu-Ta interfacial sliding. The Ta stresses in the SiO_2-Cu structure changes from tensile to compressive for all w/t aspect ratios.

Stresses normal to the dielectric-Ta interface are not significantly affected by the Cu-Ta sliding in either interconnection system.

The effect of Cu grain boundary sliding on the Cu-Ta sliding and the relaxation of shear stress in the BCB-Cu system with large aspect ratio and thin Ta liner was also investigated. The Cu grain boundary sliding have no significant impact on the Cu-Ta sliding and its effect on the relaxation of the interfacial shear stress is also small.

A finite element technique was used to model the classical *Nabarro-Herring* creep deformation in a 1 μm square copper grain subjected to biaxial normal stresses of ± 10 MPa at 800 °C. A previously proposed finite element procedure, which used the new vacancy concentration at the boundary to predict the creep deformation of the grain, was re-evaluated and modified to improve its performance. The previous result was shown to be three orders of magnitude lower than that predicted by the analytical model. The new finite element procedure, which predicts the creep deformation of the grain using the nodal displacements computed based on the components of vacancy flux at the nodes, was shown to be capable of modeling the *Nabarro-Herring* creep phenomenon satisfactorily. The finite element result agrees with the prediction of the classical *Nabarro-Herring* creep model within a factor of two.

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