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# A Prototype ASIC for APD Array Readout of Scintillating Plastic Fibers

John R. Macri, Alan Wintenberg, Mark Widholm, Usha Jagadish, James Ledoux,
Mark L. McConnell, S. Shane Frank and Hansford Cutlip

*Abstract--* **We report on the development of custom front-end electronics for use with avalanche photodiode (APD) arrays as part of a NASA technology study for the readout of scintillating plastic fibers. APD arrays featuring 64 1 mm square pixels are used. We demonstrate that a pixel of these APD arrays coupled to relatively thin (0.25 mm) and short (15 cm) scintillating plastic fibers can be used to detect and measure the tracks of even minimum ionizing particles (MIPs). An application-specific integrated circuit (ASIC) implementation of the electronics is required to produce a detector sufficiently compact for practical use in a flight experiment featuring many thousands of channels. This paper briefly describes the detector concept and performance and presents the design and performance of a four-channel prototype ASIC fabricated using the 0.35 micron TSMC process.**
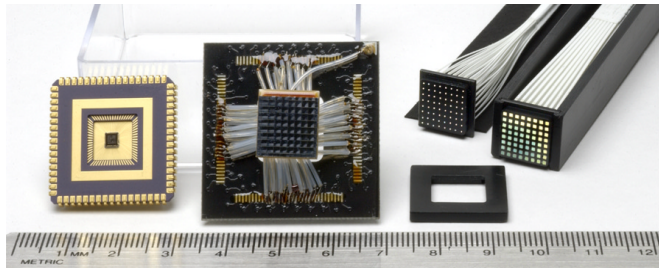
Fig. 1. Packaged ASIC, APD array and scintillating fiber bundles.

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## I. DETECTOR CONCEPT AND DEMONSTRATION

This development effort focuses on the SOlar Neutron TRACking experiment (SONTRAC). The SONTRAC detector measures the direction and energy of incident 20 to 250 MeV neutrons by recording the tracks of the ionizing recoil protons in a closely packed bundle of scintillating plastic fibers. For proton tracking at 20 MeV SONTRAC requires scintillating plastic fibers ≤0.25 mm thick. The scintillating fiber and APD array combination is also under study for application in high energy gamma-ray telescopes that track minimum-ionizing electron-positron pairs. Reports on the SONTRAC detector and on the planar processed APD arrays used here were presented previously [1]-[3].

Fig. 1 shows a photograph of a prototype APD array and two small bundles of closely packed scintillating plastic fibers used in this study. The packaged ASIC is shown at the left. The windowless APD array (center) is bonded to a ceramic carrier with the signal leads emerging from the bottom and fanned out to the pads of a PGA adapter for insertion into the test box. Both the APD pixels and the scintillating fibers are formed in 8×8 arrays. A plastic cookie and collar (lower right) are used to match and align the fibers with the 1.27 mm pitch APD pixels. Fibers with square cross sections of 0.25 mm (left) and 0.75 mm (right) were used in this study.

Two sets of data were collected to demonstrate the performance of the scintillating fiber/APD detector for the SONTRAC application and to help define specifications for the ASIC: 1) 65 MeV protons incident on 0.75 mm fibers at room temperature and 2) Beta particles from a $^{90}$Sr source incident on 0.25 mm fibers at -32°C. These measurements were conducted by the University of New Hampshire (UNH) using commercially available electronics.

A bundle of 0.75 mm square fibers with APD array readout was exposed to a beam of 65 MeV protons to demonstrate proton track recognition performance at room temperature. Aluminum attenuators were placed between the beam and the fibers to provide lower energy protons to simulate the end-of-track signal. Fig. 2 shows a composite of measured and simulated results. Note that pulse height resolution is adequate for recognition of the Bragg peak near the end of the ionization track as required to determine proton direction. Note also that the measured peak widths exceed those of the
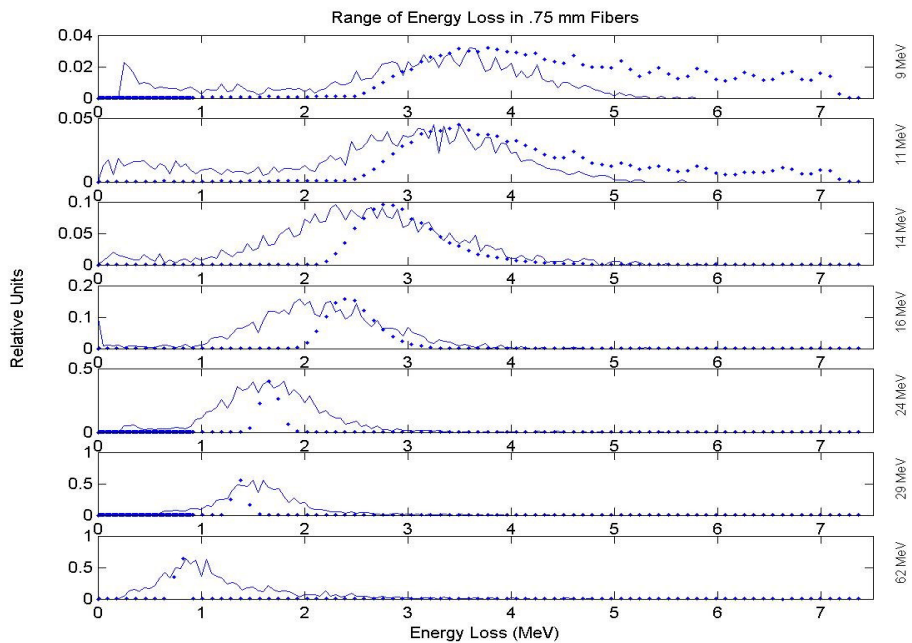
Fig. 2. Composite of measured (lines) and simulated (dots) data showing APD response to a range of proton interaction energies in 0.75 mm scintillating fibers. The measurements were made at room temperature.

simulated ionization losses. This *excess noise* effect derives from a statistical distribution in the APD gain for each photoelectron [4].
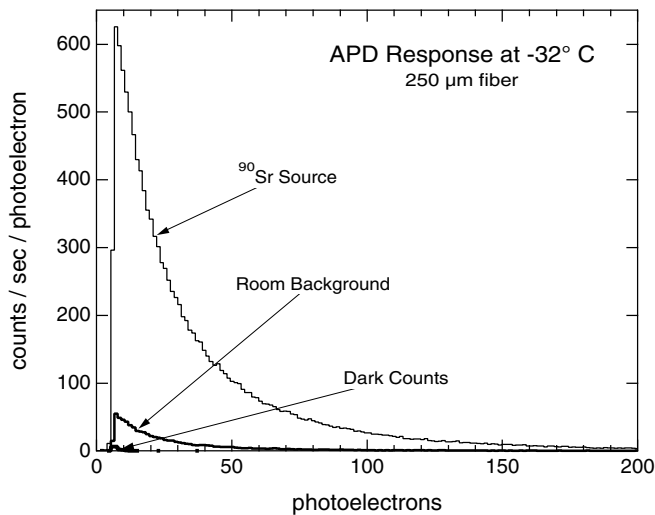


Fig. 3. Scintillating fiber / APD response to minimum ionizing particles measured at -32°C.

Fig. 3 shows the APD response to scintillations in a 0.25 mm square, 15 cm long fiber. The multi-clad fibers were specially formulated by Saint-Gobain using a 3HF dye concentration appropriate to the fiber dimensions and white EMA. A Mylar reflector on the far end of the fiber was employed to enhance light collection. The APD was cooled to -32° C and operated at a gain of 1300. Cooling reduces APD leakage current and associated noise and permits the use of higher APD operating gains. With the trigger threshold set equivalent to ~4 primary electrons the dark count rate was less than 20 triggers/s. The fiber was exposed from the side to beta radiation from a $^{90}$Sr beta source ($E_{max} = 2.3$ MeV). Fig. 3 shows the dark count spectrum as well as that of the fiber exposed to room background and to this source.

We estimate that 50 photoelectrons are created in the APD for a minimum ionizing particle (MIP) traversing the 0.25 mm thickness of the scintillating plastic fiber. Electronic noise (FWHM) was measured to be equivalent to 3 primary electrons (3900 electrons at APD output) with a test pulse (not shown). We estimate that the scintillation signal in a fiber / APD pixel from a recoil proton at the top end of SONTRAC's energy range (250 MeV) would be ~2 MIPs or 100 photoelectrons. The maximum signal, at the end of a proton track, would be ~46 MIPs or 2300 photoelectrons.

These results demonstrate the ability of the scintillating fiber / APD combination to detect and locate the tracks of even minimum ionizing particles and to determine the direction of protons as required for SONTRAC.

In addition to these demonstrated capabilities, the APD ASIC readout electronics for SONTRAC must be compact and low power level to serve the approximately 100,000 closely packed scintillating fiber channels composing a flight detector.

## II. ASIC REQUIREMENTS, PROTOTYPE DESIGN AND STATUS

The prototype APD ASIC for SONTRAC was designed as a tiny chip featuring four self-triggering channels and sparse readout.

### A. Summary of Requirements and Status

Table 1 lists important requirements of the prototype ASIC and summarizes the performance status.

### B. Design

The detailed design and simulation of the prototype APD ASIC was conducted at Oak Ridge National Labs (ORNL). Fig. 4 is a block diagram of the ASIC. Fast (<10 ns) signals are presented to the ASIC from the pixels of an APD array. The ASIC has multiple channels each consisting of a charge-sensitive preamplifier, shapers, discriminator and associated controls. The prototype ASIC has four channels; ultimately, 64 will be needed to match each 8×8 APD array.

TABLE I

| Item | Requirement or Goal | Status |
|---|---|---|
| Charge sensitive preamplifier, 2 stage shaping | 1 per APD pixel. 4 channels on prototype ASIC. | 4 ch., incl. 1 spy ch. Spy ch. not working |
| Range of input signals (low gain setting) | $5 \times 10^3$ to $1 \times 10^6$ electrons (0.8 to 160 fC) | Measured linear to 180 fC |
| Range of input signals (high gain setting) | $1 \times 10^3$ to $1 \times 10^5$ electrons (0.16 to 16 fC) | Measured linear to 25 fC. |
| Trigger and trigger walk | Self-triggering on first (fast) gain stage. Walk <100 ns across dynamic range | Trig. & walk verified only in 40 to 160 fC range. |
| Peaking times: (2 stages) | $1^{st}$: 50-100 ns, $2^{nd}$: ~ 150 ns, combined: 200 ns | Measured combined= 610 ns. |
| Sample and hold | 1 per pixel | Verified |
| Analog MUX | Common | Verified |
| Readout discriminator | After mux, allows sparse readout. Adjustable threshold | Verified |
| Channel enable (1 per pixel) | Digital bit to shutdown an individual channel | Verified |
| Pulse heights | Serial readout of all channels exceeding readout threshold | Verified |
| Noise | <2000 electrons rms | 1850 electrons rms |
| Threshold | Adjustable down to 5000 electrons (0.2 MIP at APD gain 500) | Discriminator not working <640,000 electrons |
| Power consumption | < 1 mW/channel | <2 mW/channel. Includes per chip overhead |
| Signal coupling and APD leakage current | DC coupling. Tolerant to leakage up to 100 na | Tested okay up to 80 na. |
| Input protection (direct detection of proton and APD breakdown | No damage to from input pulse $<10^{10}$ electrons or APD pixel breakdown | Verified |
| Gain variation among channels | < 5% | Verified (spy ch. not working) |
| Cross talk for full scale pulse | < 5% | < 2% |
| Temperature coefficient of gain | < 0.1%/°C | < 0.2%/°C |
| Sparse readout | Readout discriminator | Verified |
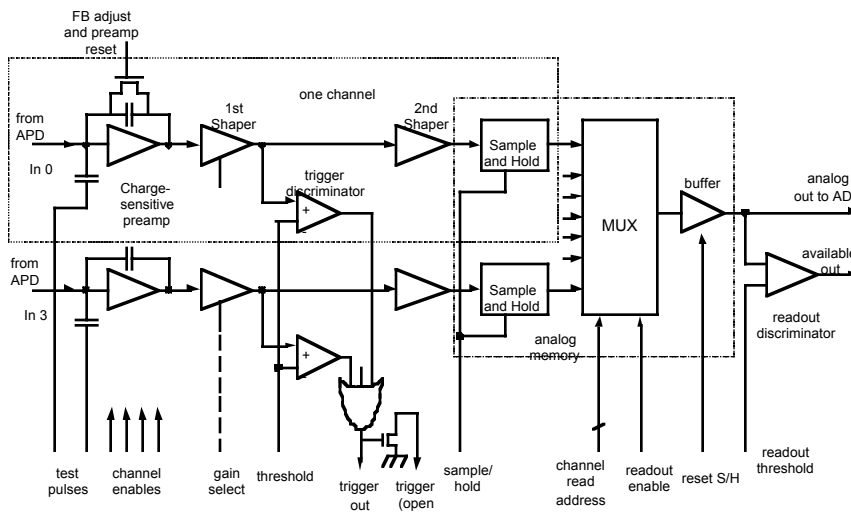
The operation of one channel is as follows. Pulses produced by an APD pixel are integrated using a charge-sensitive preamplifier and then shaped in two stages. A discriminator following the first shaping stage has a programmable threshold and is used to detect the leading edge of pulses. Its output is logically OR'ed with that of all other discriminators, and that result is sent to the system-level trigger logic. The second shaping stage passively filters the pulse and increases the peaking time to approximately 200 ns. The sample-and-hold circuit, controlled by the external trigger logic, holds the peak of this signal. *A key feature of this design is that all pixels are sampled simultaneously and held as analog values.* Once an event has triggered the system, the readout phase starts. The system controller, which is not part of the ASIC, uses the multiplexer to sequentially send the output of each sample-and-hold to the analog output and to the readout discriminator. If the signal is above the threshold of the readout discriminator, then it is digitized by the ADC, but if is below the threshold, the system controller skips digitizing that channel and proceeds to readout the next one. The prototype uses an off chip ADC but this function would be moved on chip for handling large arrays.

The preamplifier and shapers are designed to operate on less than 0.5 mW and to have no more than 500 electrons (rms) noise for a 2 pF detector. The charge sensitive preamplifier has a gain of 5mV/fC and is followed by a programmable voltage gain stage that does double duty as the first shaping stage. Gains of 1.6V/V (low gain setting for the bigger test pulses) or 12V/V (high-gain setting for the actual charges expected) are possible. The first pulse shaper is approximately CR-RC with a peaking time of approximately 70 ns.

To save power, a passive shaper is used for the second stage. The passive shaper consists of a simple RC filter with the C being part of the sample and hold, which is an analog memory [5]. The nominal peaking time is 220 ns when processing the pulse developed by the first shaping stage. The first pair of switches (Fig. 5) is opened to allow capturing the peak (hold mode). The second pair of switches is normally open and is closed to allow reading of the held peak.
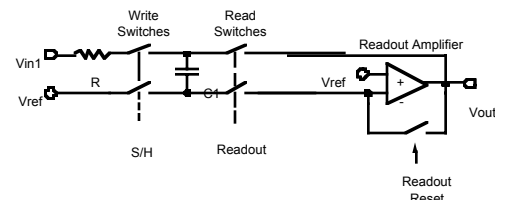
Fig. 5. Analog memory.

In an array detector that is designed to capture multi-channel, simultaneous events, it is possible to combine information from several channels in real time and to use that information to trigger sampling of all channels. By combining the information and not sampling any channels unless the

Fig. 4. SONTRAC prototype ASIC block diagram.

predetermined conditions are met, only events that are potentially of interest are captured, and the probability of the event being interesting is increased. An additional benefit of this type of triggering is the sampling of channels that would have signals insufficient to self-trigger.

For SONTRAC, we can operate on the assumption that events of interest will have a proton end-of-track (Bragg peak) signal in at least one channel. Since this is a large signal, it will be well above the noise and relatively easy to discriminate. The basic idea is to set the discriminator threshold to a level that is a relatively small fraction of the end-of-track signal, but well above the noise. This should give a time mark (logic pulse) delayed by a small fraction of the first shaper peaking time (150ns). The outputs of all the discriminators on a single chip are OR'ed together and sent to the detector trigger logic (which might OR all chip OR-outputs together.) to produce a system trigger. The system trigger would be an input to the chip and would be delayed to cause the sample-and-hold circuit to go into hold mode just as the output of the second shaper peaks.
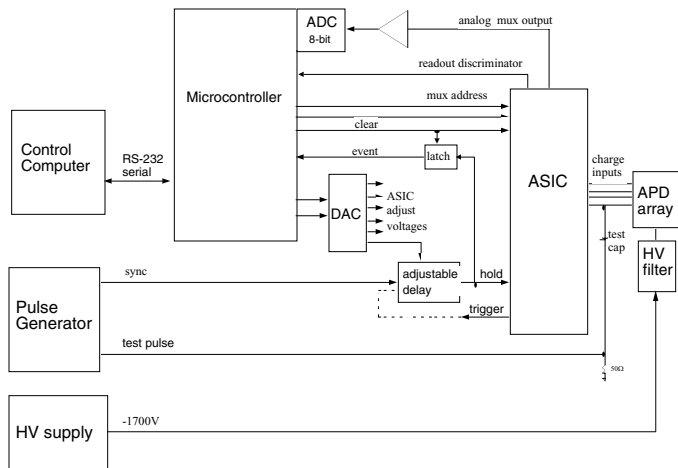


Fig. 6. APD test fixture.

## III. ASIC TEST CONFIGURATION

The ASIC test apparatus was designed and built at UNH. Fig. 6 illustrates the APD ASIC test setup. All functions shown except for the HV supply and the pulse generators are enclosed in one test fixture. The test fixture supports an APD array and four prototype ASIC chips for readout and permits external adjustment of key biases and shaping parameters as well as control of the discriminator levels and implementation of the external, system-level, trigger. Test pulses can be applied independently to each channel and the performance at important nodes of the circuit can be examined for the prototype chip's spy channel. The test fixture fits into an environmental chamber for cooling.

As problems were encountered with the ASIC's spy channel and fast trigger circuit, tests with the prototype ASIC have been limited to the stimulus of the APD with a pulsed light source and to the ASIC preamp with a test pulse generator.

## IV. APD ASIC TEST RESULTS

Testing of the prototype ASICs was conducted at UNH. Tests of the fast trigger circuit were performed at ORNL.

### A. Charge Gain, Linearity and Dynamic Range

The charge gain was measured by using a known external test capacitance. The external test capacitor was mounted with ground plane shielding to minimize any stray coupling into the preamp input lead. The capacitor has a 10% tolerance and the input voltage was measured to about 5%. The test board has an internal test pulse wired directly to the ASIC pins. The coupling from this input into the preamp is dominated by the pin-to-pin capacitance of the ASIC packaging so its value isn't well known. The external capacitor was used to calibrate this input.

The pulse height peak channel was recorded for several different test pulse voltages using the external and internal test. The internal test matches the external one if you assume a capacitance of 1.93pF. This is a reasonable value for pin-to-pin coupling in this setup.

The data (Fig. 7) shows a linear response for the high gain range in the 6 to 25 fC range. The response to test pulses changes slightly with the APD detector connected and biased. The low gain range appears to have somewhat worse linearity than the high gain range (not shown).
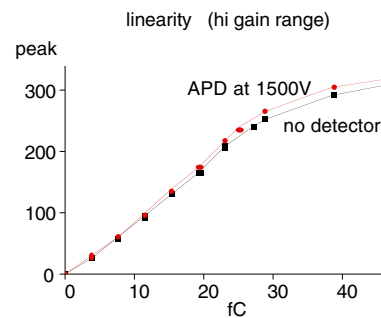


Fig. 7. Charge gain and linearity

### B. Pulse Shaping

Fig. 8 illustrates the pulse shaping as measured by varying the delay between the externally generated test pulse and the hold signal applied to the ASIC. The measured peaking time, 610 ns, is triple the 200 ns design goal. Some of this discrepancy has been accounted for by measuring the value of the resistor in the second stage shaper. It measures 373 kΩ, considerably more than the 217 kΩ value given by the layout/extraction tool. With this



Fig. 8. Pulse shaping.

measured value we should get about 373 ns for the peaking time. Further study is required to understand the remaining causes of this discrepancy.
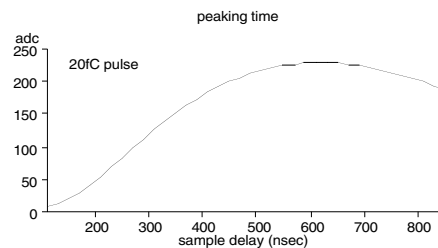
## C. Trigger

We were only able to measure performance of the internal fast trigger function for very high discriminator level settings and large input pulses in the low gain mode. The delay between the input and the trigger output was about 40ns vs. 20-30ns expected from the simulation. We verified that the trigger walk meets its design specification for the 40 fC to 160 fC portion of its dynamic range.

Laboratory tests suggest that the problem with the discriminator is inadvertent feedback. When the discriminator fires, the logic output feeds back to an earlier stage and adds to the signal, causing the discriminator to fire again. This may have been avoided had we made the trigger output a current mode or low voltage differential output.

## D. Noise and Optimum Operating Conditions

Fig 9 shows the measured electronics noise width of an ASIC channel. The amplifier noise is 0.3fC rms with no detector and increases with increasing APD bias. This increase is due to APD dark current noise and can be reduced by cooling the APD. Operation at 1700V, 25°C corresponds to a gain of 400 and a dark current of 80nA.



Fig. 9. Measured noise with no detector (top) and with the biased APD

Fig. 10 shows the dark noise and response of an APD pixel / ASIC channel to a calibrated pulsed light source measured with the APD gain set at 450 and at two operating temperatures: 25°C and 0°C. The lower end of light pulse intensity, 50 photoelectrons, was chosen to reflect the scintillation signal expected from a minimum ionizing particle (1 MIP).

Note that the response to the light pulses is significantly broader than the electronics noise. Again, this is mostly due to statistical gain variation in the APD device [4]. The measured APD gain distributions are roughly +-25%. This percentage width is



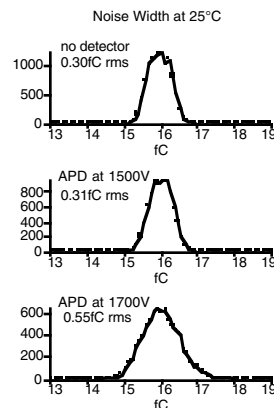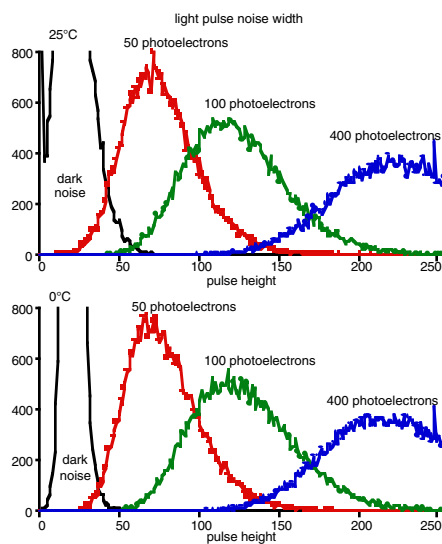Fig. 10. Measured APD / ASIC signal and noise at APD gain of 450.

relatively independent of bias and temperature. It improves somewhat at lower temperatures and broadens significantly when the APD is run near its maximum gain.

An APD gain of around 450 provides the best separation between the dark noise and the minimum signal at room temperature. Increasing the gain beyond this point broadens both the dark current peak and the minimum signal peak. Cooling the APD decreases the dark current noise, which results in less overlap. This will permit the setting of a lower readout discriminator threshold.

## V. CONCLUSIONS AND FUTURE WORK

We have demonstrated that the scintillating fiber / APD detector generates ample signal for the SONTRAC application when operated at -32°C and an APD gain of 1300. Further analysis and measurements suggest that a sufficient signal to noise ratio for the detection of minimum ionizing particles in 0.25 mm fibers would be achieved at 0° C and with APD gain set well below breakdown.

We have designed, fabricated and tested first prototype ASIC devices for readout of APD arrays. While the self-triggering feature of these chips is not working for small signals other important performance parameters have been verified to be in compliance with the requirements. These include charge sensitivity, noise and linearity across the specified dynamic range, tolerance to APD breakdown and compatibility with high leakage currents facilitating testing at room temperature.

Further study is required to understand the larger than expected peaking time. Further study and redesign of the ASIC fast discriminator circuitry are required to address the inadvertent feedback problem. We will seek new funding to address these issues and extend the development to include compact APD/ASIC packaging as would be required by SONTRAC and other many-channel instruments.

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